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Impact of Junction Non-abruptness on Random Discrete Dopant Induced Variability in Intrinsic Channel Tri-gate MOSFETs

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1. Introduction

As the gate length (L_g) of MOSFETs is scaled to nanoscale dimensions, variability induced by random dopant fluctuation (RDF) is projected to be a serious problem [1]. The use of intrinsic channel in MOSFETs becomes preferable due to its significant advantage to largely suppress the impact of RDF [2]. However, it is difficult in process to form abrupt source/drain (S/D) junctions because of unavoidable diffusion of dopants from highly doped S/D regions into the undoped channel region. The straggle of dopants provides a source of RDF in the channel. N. D. Akhavan et al have studied the impact of junction non-abruptness (JNA) on the RDF induced variability [3]. However, they assumed a fixed number of dopants in the channel that located at a fixed distance from the S/D junctions, which is not realistic. Thus a systematical study that takes into account the realistic dopant distribution is desirable to achieve an accurate estimate on the JNA impact affecting device variability. In this work, we use statistical TCAD simulations to explore the impact of JNA on RDF induced variability in intrinsic channel SOI tri-gate MOSFETs. The results can be help in the optimization of the Tir-gate MOSFET and its related ICs.

2. Device structure and simulation method

Fig. 1 shows the structure of the simulated SOI tri-gate MOSFETs, with their parameters listed in **Table I**. **Fig. 1**(a) also illustrates the dopants straggling into the intrinsic channel region. Only these straggled dopants are treated randomly and discretely, while others in the highly doped S/D and extension regions are handled with conventional jellium model. The realistic dopant distribution in the channel is determined according to the requirements by ITRS on junction lateral abruptness [4], which specifies the decay length (L_{dec}) over which the doping concentration fall 1 decade. In ITRS, L_{dec} value of $0.1L_g$ is required. In this work, we use L_{dec} values of $0.1L_g$ and $0.2L_g$ to study the impact of process on variability. The channel doping profile is discretized so that the dopant number fulfills the Poisson distribution [5] and their positions are completely randomized.

3D atomistic drift-diffusion (DD) simulator with density gradient (DG) quantum corrections is used in this work. **Fig. 2** plotted the simulated linear and saturation transfer characteristics of the same 20nm intrinsic tri-gate MOSFET using both the DD and our 3D Monte Carlo (MC) simulator [6]. The perfect match shows the feasibility of the DD simulator on such scale of the devices, especially in the region of lower V_{ds}. In the following, each device type is simulated with an ensemble size of 100.

3. Results and Discussion

Fig. 3 shows the saturation (V_{ds}=0.8V) and linear (V_{ds}=0.05V) transfer characteristics of the 20nm tri-gate MOSFET under different L_{dec} of 2nm and 4nm. Obvious current variation can be observed in both cases. As process deteriorates, device variability increases rapidly, especially in the subthreshold regime. These can be reflected in the variation of threshold voltage (V_{th}), as plotted in **Fig. 4**, and the variation of subthreshold slope (SS), as plotted in **Fig. 5**. When L_{dec} changes from 2nm to 4nm, the standard deviation (σ) of V_{th_lin} increases from 5.7mV to 29.4mV, while σV_{th_sat} increases from 8.6mV to 40.5mV. This indicates that V_{th_sat} is more susceptible to JNA. In **Fig. 4** we can also observe the variation of DIBL, which is defined as $(V_{th\_lin}-V_{th\_sat})/0.75$. The distribution of SS also spreads out, with σ increasing from 1.37mV/dec to 5.90mV/dec. Besides the subthreshold regime, **Fig. 6** further reveals the non-negligible variation of the on current (I_{on}). Although more straggled dopants in the channel can slightly improve the average I_{on}, the variation and the mean value of the I_{on}/I_{off} ratio are both severely degraded. **Fig. 7-9** further summarized the dependence of JNA induced variability on device scaling. As the gate length shrinks, device variability increases quickly, even when devices with different L_g have retained the same L_{dec} criteria, e.g. $0.1L_g$. What can be learn more from **Fig. 7-9** is that if process deteriorates, (which is very possible in the future since the $L_{dec}=0.1L_g$ requirement is very difficult to follow as the device further scales down) devices with smaller L_g are more susceptible to the process change. **Fig. 10** shows the scatter plot of the saturation I_{on} versus straggled dopant number in the channel. The dependence of I_{on} on channel dopant number increases with L_g decrease, which can be deduced from the increase of the slope of the linearly fitted lines shown in the figure. This indicates that the fluctuation of the dopant number as well as their positions can influence the I_{on} variation, showing the importance of a realistic dopant distribution. I_{on} also exhibits strong correlation with V_{th} regardless of the different L_g and L_{dec}, as plotted in **Fig. 11**. This can be useful for the compact model concerning JNA induced variability.

4. Summary

3D statistical TCAD simulations on the impact of JNA on RDF induced variability in intrinsic channel SOI tri-gate MOSFETs are performed. Results show that JNA can lead to substantial variability, and devices with smaller L_g are more susceptible to JNA. Results also indicate the importance of a realistic dopant distribution for an accurate estimate of the JNA impact.

References

[1] S. Markov, et al. EDL, **33**(3), 315, 2012. [2] S. Chouksey, et al. TED, **56**(10), 2348, 2009. [3] N. D. Akhavan, et al. SOI 2011. [4] www.itrs.net, 2011. [5] N. Sano, et al. Microelectronics Reliability, **42**, 189, 2002. [6] K. L. Wei, et al. SSDM 2011.

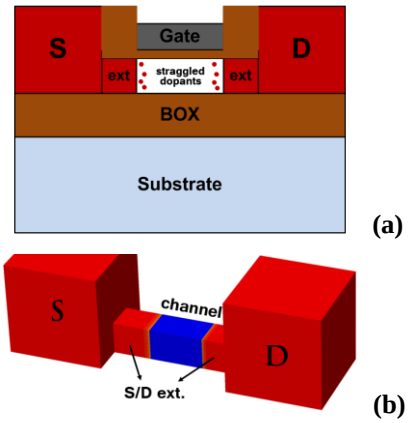

Fig. 1 Structure of the SOI tri-gate MOSFET: (a) cross section of the entire device with straggled dopants in the channel shown; (b) 3D view of the active region.

PARAMETERS	VALUES
Gate length (L_g)	20 ~ 50 nm
Channel width (W)	10 nm
Channel height (H)	10 nm
BOX thickness (T_{BOX})	50 nm
S/D ext. length (L_{ext})	10 nm
EOT	0.9 nm
S/D doping	10^{20} cm^{-3}
Ext. doping	10^{20} cm^{-3}
Channel doping	Intrinsic

Table I Parameters of the SOI tri-gate MOSFET used in simulation.

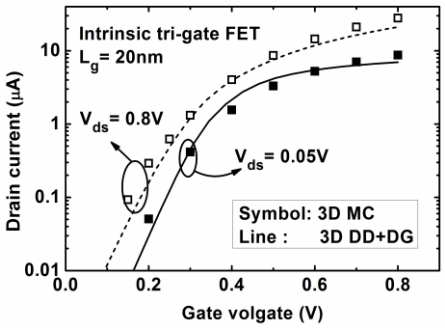

Fig. 2 Comparison of the 3D MC and DD simulated linear (V_{ds}=0.05V) and saturation (V_{ds}=0.8V) transfer characteristics of the same 20nm intrinsic tri-gate MOSFET.

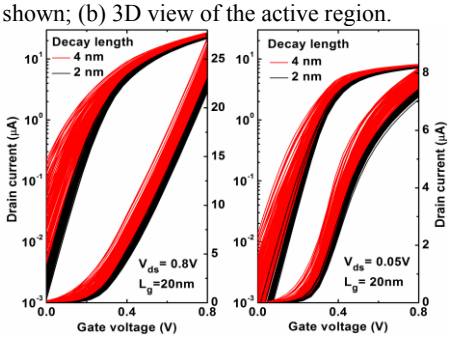

Fig. 3 Saturation (V_{ds}=0.8V) and linear (V_{ds}=0.05V) transfer characteristics of the 20nm tri-gate FETs under different doping decay length of 2nm and 4nm.

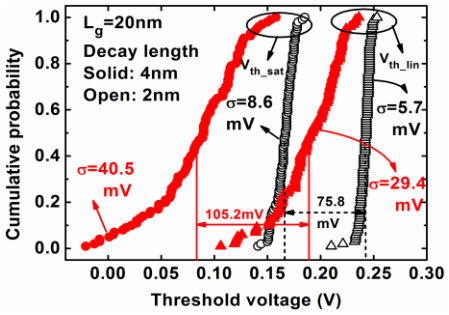

Fig. 4 Threshold voltage distribution of the 20nm tri-gate FETs under different doping decay length of 2nm and 4nm.

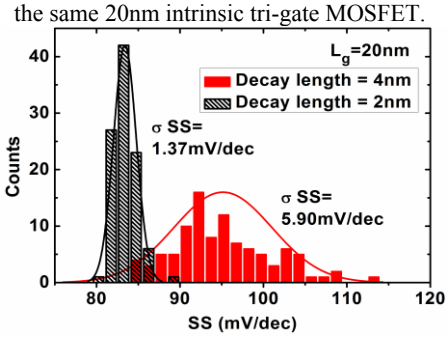

Fig. 5 SS distribution of the 20nm tri-gate FETs under different doping decay length of 2nm and 4nm.

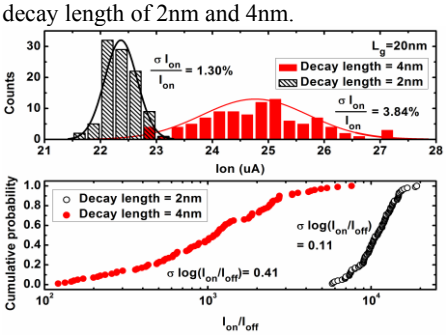

Fig. 6 On current (up) and I_{on}/I_{off} ratio (down) distribution of the 20nm tri-gate FETs under different doping decay length of 2nm and 4nm.

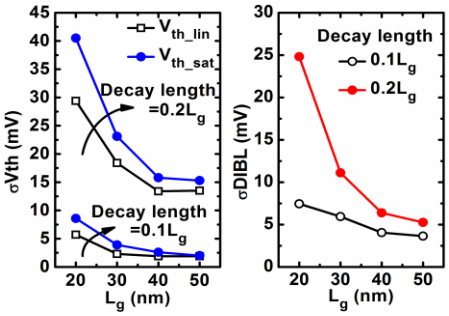

Fig. 7 Evolution of the V_{th} (left) and DIBL (right) variation with the scaling of SOI tri-gate FETs.

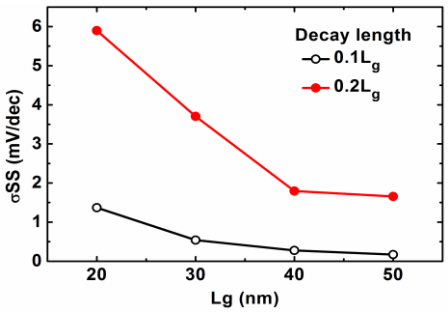

Fig. 8 Evolution of the SS variation with the scaling of SOI tri-gate FETs.

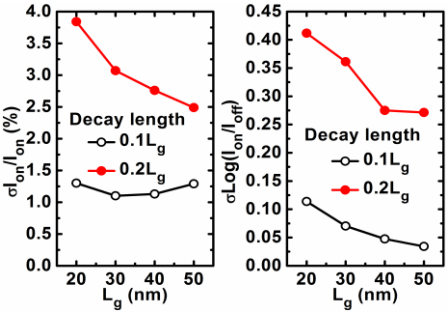

Fig. 9 Evolution of the I_{on} (left) and I_{on}/I_{off} ratio (right) variation with the scaling of SOI tri-gate FETs.

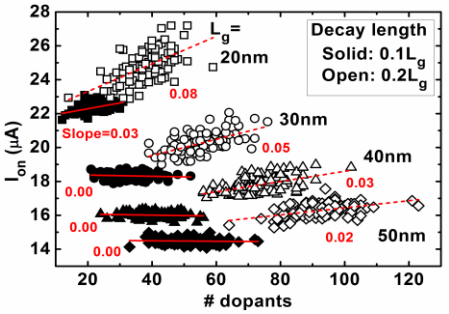

Fig. 10 Scatter plot of saturation I_{on} versus the straggled dopant number in the channel. The Ion dependence on channel dopant number increases with L_g decrease.

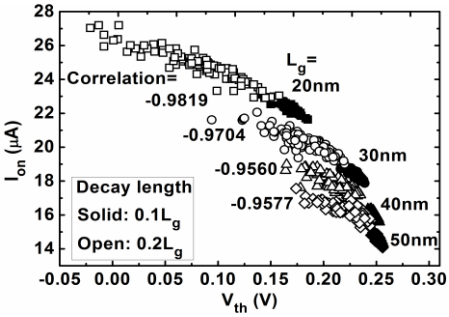

Fig. 11 Scatter plot of saturation I_{on} versus saturation V_{th}. I_{on}-V_{th} correlation is obvious for devices with various channel lengths and doping decay lengths.