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2D and 3D Fully-Depleted Extension-less Devices for Advanced Logic and Memory Applications

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Abstract

In this work we explore the use of extension-less doping schemes for fully-depleted devices [2D: ultra-thin body and BOX (UTBB) planar devices; 3D: FinFETs on bulk-Si or SOI substrates], suitable for advanced logic, memory and dense circuit applications. We demonstrate that by using Si-epitaxial raised S/D (SEG) followed by HDD-only implantations (I/I), or by using doped-SEG and no I/I: 1) lower I_{OFF} and DIBL; 2) steeper sub-threshold slope (SS); 3) higher I_{ON}/I_{OFF} ratio; and 4) higher retention times (UTBB-FBRAM) can be obtained, while reducing cost & cycle time with less critical I/I photos. SEG facet formation can be controlled by the spacers shape and epi pre-clean step and its impact on device characteristics for logic and FBRAM applications is also analyzed.

Introduction

Ultra-thin body fully-depleted devices [planar on ultra-thin BOX (UTBB) and FinFET-based multi-gate structures (MuGFETs)] have long been considered an attractive option for enabling further CMOS scaling beyond the 22nm technology node, thanks to their improved electrostatics and steeper sub-threshold slopes (SS), with reduced V_T variability due to lower channel dopants concentration [1-8]. For both architectures, however, the extremely thin body poses new integration challenges, namely for junction engineering and the extendibility of conventional doping techniques such as ion implantation (with tilt angle restrictions due to resist shadowing at tight pitch), parasitics and series resistance ($R_{S/D}$) control. Improved morphology of the c-Si body and near zero-tolerance Si loss is required. In this paper, several extension-less strategies for scaled UTBB and FinFET devices are evaluated for improved performance, short-channel-effects (SCE), and variability control. Increased interest in potential memory architecture alternatives to DRAM, such as one-transistor floating body RAM (1T-FBRAM) [9,10], will also be addressed in this work through the use of a process flow fully compatible with UTBB logic technology.

Device fabrication

A schematic of the process flow used for fully-depleted devices fabrication is shown in Fig.1, for both 2D (UTBB planar) and 3D (FinFETs on bulk-Si or SOI substrates). Extension-less devices were fabricated with a narrower 1st spacer (CD≤15nm after SEG) followed by SEG → HDD I/I → RTA as illustrated in Fig.2. An alternative I/I-free approach consists in doing doped-SEG → RTA. Reference devices include extensions I/I prior to SEG → HDD I/I → RTA, for both 2D and 3D architectures, with total spacer width prior to silicidation similar for all devices. Gate stack consists of (HfSiON or HfO_2)/TiN for logic, 5nm SiO_2/TiN for 1T-FBRAM.

Device results and discussion

Fig.3 shows lower I_{OFF} values for extension-less SOI-FinFET devices, consistent with the expected reduced gate overlap. 7°tilt I/I was used here for all devices under comparison to enable pitch scaling without resist shadowing effects. These devices also exhibit excellent SCE behavior with the I_D-V_G curves in Fig.4 highlighting the lower off-state current obtained with extension-less (SEG → HDD I/I → RTA) *vs.* reference (Extension I/I → SEG → HDD I/I → RTA) implant strategies, corresponding to a lower DIBL~36mV/V and SS~70mV/dec. Furthermore, it is important to mention the better quality, defect-free SEG (⇒ less R_{out} variability) expected to be obtained when starting from undoped fins [3,5], as is the case with the extension-less I/I approach. An alternative extension-less and I/I-free doping technique is illustrated in Fig.5, where a RTA anneal is used to drive dopants from the in-situ doped-SEG grown on the S/D areas of a bulk-FinFET device. The RTA condition used determines the dopant (As in Fig.5) diffusion profile and resulting doping contours in the top and vertical channels. Benchmarking with reference devices (bulk-FinFETs with conformal doping by I/I), TCAD simulations were performed for assessing the impact of several process parameters changes, such as spacer width variations, on junctions profile and device characteristics. Overall, as observed before for extension-less devices built with [SEG → HDD I/I → RTA], steeper SS, smaller DIBL, lower I_{OFF} and higher I_{ON}/I_{OFF} ratio values are also obtained for these I/I-free devices (Figs.6,7). Wider offset (1st) spacers translate into reduced gate overlap and a further increase on the difference for these parameters with regards to the implanted-reference, with a compromise needed to also keep high absolute values for I_{ON}. Fig.8 shows that increasing the Si-recess depth (10 → 40nm) prior to SEG growth leads to higher drive currents due to a more effective fin doping, but at the expense of a reduction in the I_{ON}/I_{OFF} ratio and a small (eventually leveling-off) DIBL increase.

TEM image and schematics of UTBB planar devices fabricated for use as 1T-FBRAM are shown in Fig.9, with ~14nm-thick Si channel and ~18nm-thick BOX. Also in this case, improved DIBL-L_{gate} behavior is measured for extension-less devices built with the I/I sequence: SEG → HDD I/I → RTA (Fig.10). Fig.11 shows devices with and without SEG faceting, depending on the spacers bottom shape and the HF time used in epi pre-clean. A faceted SEG in S/D has been shown to reduce $R_{S/D}$ and minimize gate-to-S/D parasitic capacitance [4,6]. Its impact on the lateral electric field for a L_{gate}~70nm device in the hold "0" state is shown in Fig.12. A lower maximum field at gate edges was simulated for extension-less devices, more so if SEG has no facets. This results in a ~5× retention time improvement for 1T-FBRAM extension-less devices with faceted SEG, with further improvement expected to occur with facet-less SEG due to its even lower maximum field (Fig.13). Retention is determined by the "0" state degradation (holes generation occurring during "0" state hold), with band-to-band tunneling and trap-assisted-tunneling mechanisms limiting the retention time [11] and responsible for the field dependence seen here. At the same time, Fig.13 shows that similar retention time distributions are obtained for the different type of devices evaluated suggesting similar traps, and generation/recombination (GR) centers distributions. For logic UTBB planar devices (see Fig.14), the two doping approaches (with and without extensions I/I) yield results in line with those obtained for FinFETs and for 1T-FBRAM UTBB devices. This is illustrated by the simulation results plotted in Figs.15 and 16. Overall, lower I_{OFF}, steeper SS, and smaller DIBL values can be obtained for extension-less devices with optimized 1st spacers width. Again, careful balance between I_{OFF} reduction and I_{ON} increase is needed, depending on final device application, including 6T-SRAM for which lower I_{OFF} values are of the uttermost importance. Figs.15,16 also show that, for similar HDD-only I/I conditions, SEG faceting results in considerably improved drive currents with no significant I_{OFF} penalty, though at the expense of higher DIBL and SS values.

Conclusions

A comprehensive evaluation of two extension-less doping schemes suitable for scaled 2D and 3D fully-depleted devices for logic and memory applications was reported: HDD-only I/I after SEG or I/I-free, doped-SEG, both followed by RTA. Results show: lower I_{OFF} and DIBL, steeper SS, higher I_{ON}/I_{OFF} ratio, and higher retention times (UTBB-FBRAM), with reduced cost & cycle time. SEG faceting control, key for parasitics and variability reduction, leads to improved performance for logic and memory.

References

[1] J. Kavalieros *et al.*, VLSI *Tech. Dig.* 2006, 62; [2] H. Kawasaki *et al.*, IEDM *Tech. Dig.* 2008, 237; [3] T. Mérelle *et al.*, IEDM *Tech. Dig.* 2008, 241; [4] K. Cheng *et al.*, VLSI *Tech. Dig.* 2009, 212; [5] A. Veloso *et al.*, IEDM *Tech. Dig.* 2009, 301; [6] K. Cheng *et al.*, VLSI *Tech. Dig.* 2011, 128; [7] A. Veloso *et al.*, *Jpn. J. Appl. Phys.* 50, 04DC16, 2011; [8] http://newsroom.intel.com/docs/DOC-2032; [9] I. Ban *et al.*, VLSI *Tech. Dig.* 2008, 92; [10] Z. Lu *et al.*, IEDM *Tech. Dig.* 2010, 288; [11] O. K. B. Lui *et al.*, *Solid-State Elect.* 41(4), 575, 1997.

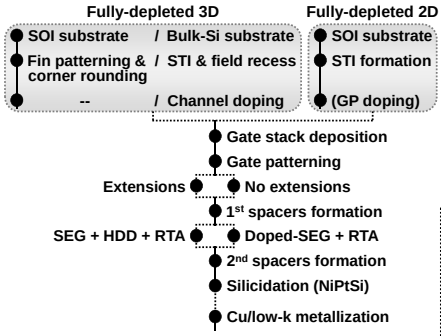

Fig.1 – Schematic of process flow used for fully-depleted devices fabrication on 300mm wafers: 3D [FinFETs with H_{Fin}~40nm on bulk-Si or SOI(145nm buried oxide)substrates], and 2D [ultra-thin body and BOX (UTBB) planar].

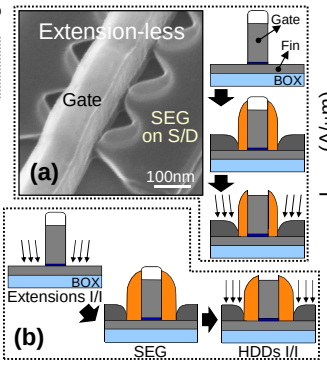

Fig.2 – Implantation schemes used for FinFET fabrication: a) extension-less devices, with SEM image after raised S/D by Si epitaxial growth (SEG) on undoped fins; b) extensions implanted prior to SEG → HDD I/I.

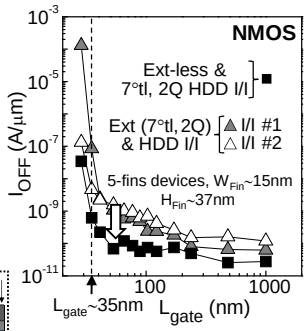

Fig.3 – Extension-less devices exhibit lower off-state current down to narrower gates (L_{gate}~35nm). They have narrower 1st spacers but a similar total(=1st+2nd) spacer width prior to silicidation.

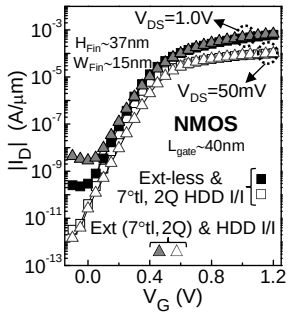

Fig.4 – I_D-V_G curves of 5-fins NMOS SOI-MuGFET devices. 20× lower I_{OFF} at similar I_{ON} for extension-less (using P HDD I/I) *vs.* reference devices (fabricated with low-tilt, double-sided As extension I/I & (As+P) HDD I/I).

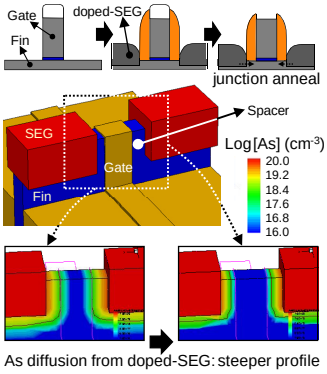

Fig.5 – On top, schematic of extension-less devices fabrication using in-situ doped-SEG for junctions formation. At the bottom, contours of net active doping for two diffusion profiles (≠ RTA) in bulk-FinFET devices.

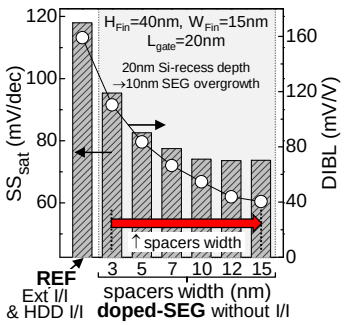

Fig.6 – Steeper SS and lower DIBL for extension-less (bulk-FinFET) devices, more so with increasingly wider offset spacers.

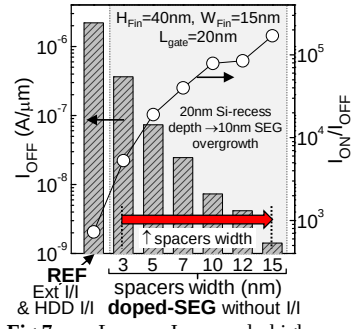

Fig.7 – Lower I_{OFF} and higher I_{ON}/I_{OFF} ratio for extension-less (bulk-FinFET) devices, more so with increasingly wider offset spacers.

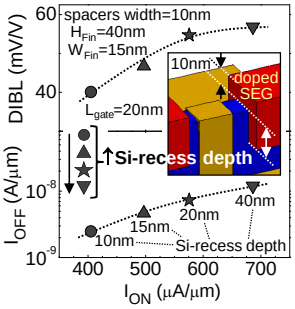

Fig.8 – Higher DIBL and drive currents (and lower I_{ON}/I_{OFF} ratio) with increased Si-recess depth prior to doped-SEG growth.

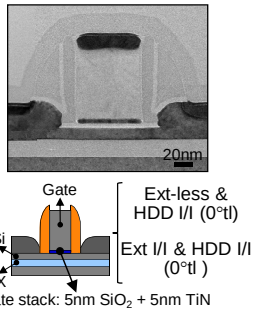

Fig.9 – TEM image and schematics of fully-depleted planar devices with ultra-thin body (UT-cSi) and ~18nm-thick BOX used for 1T-FBRAM fabrication.

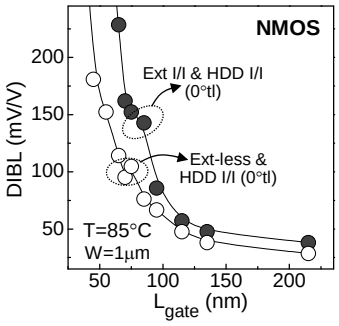

Fig.10 – Improved DIBL-L_{gate} for extension-less (P HDD I/I) *vs.* reference [As extension I/I & (As+P) HDD I/I] UTBB planar devices built for 1T-FBRAM (~14nm c-Si; ~18nm BOX; gate stack: 5nm SiO_2/5nm TiN).

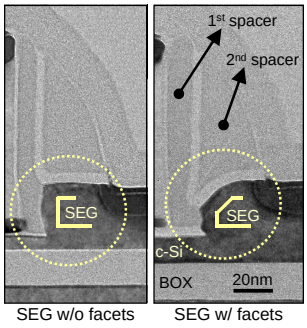

Fig.11 – X-section TEM images show epitaxial Si growth on the source and drain regions with (on the right) or without (on the left) facets, depending on the spacers shape at the bottom and epi pre-clean used.

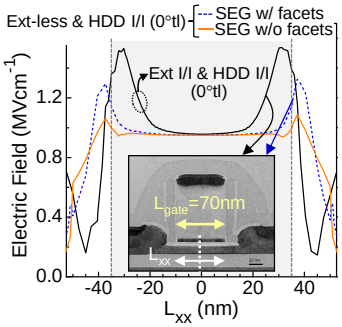

Fig.12 – Lateral electric field simulated in the hold "0" state (V_G= -2.5V, V_B=2.5V and V_S=V_D=0V) for L_{gate}~70nm UTBB-FBRAM devices. Maximum field lower for extension-less devices with SEG w/o facets.

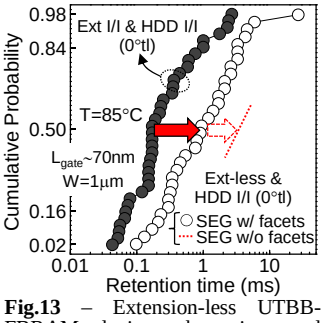

Fig.13 – Extension-less UTBB-FBRAM devices show improved retention times (data shown for L_{gate}~70nm). Further improvement expected by using SEG w/o facets.

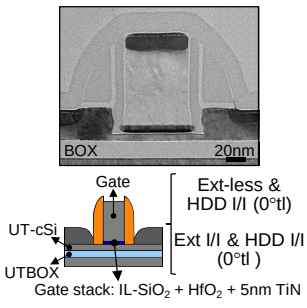

Fig.14 – TEM image and schematics of fully-depleted planar devices with ultra-thin body and ~18nm-thick BOX fabricated for logic applications.

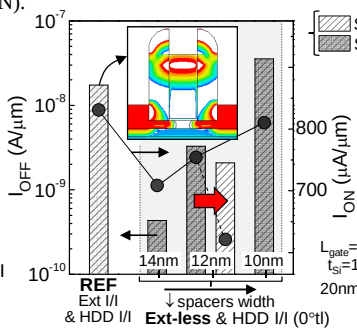

Fig.15 – Lower I_{OFF} for extension-less (UTBB logic) devices, more so with increasingly wider offset spacers. Using SEG w/ facets ⇒ higher I_{ON} with 0°tilt HDD-only I/I.

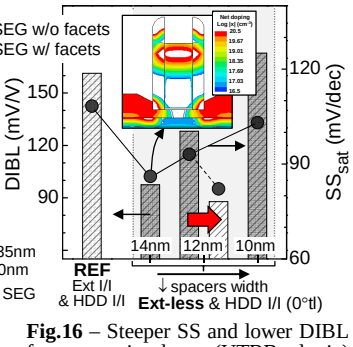

Fig.16 – Steeper SS and lower DIBL for extension-less (UTBB logic) devices, more so with increasingly wider offset spacers. Using SEG w/o facets ⇒ smaller SS and DIBL values with 0°tilt HDD-only I/I.