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The impact of Side Surface Roughness on Carrier Mobility in Tri-Gate Silicon Nanowire MOSFETs

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1. Introduction

Along with the progress in device scaling, a nanowire (NW) MOSFET has drawn much attention recently for being promising candidate of future device structures [1-3]. Since mobility is one of the most important physical quantities determining MOSFET performances, mobility behaviors of NW MOSFETs have been discussed [4-6]. Recently, we have successfully extracted the carrier mobility in "single" silicon NW MOSFETs [7], instead of multiple NW array, for more detailed analysis of NW mobility. It has been found that the NW mobility degrades as decreasing NW width. Although similar mobility degradation has also been observed by many authors, the physics mechanisms behind the mobility degradation in narrower NW have not been thoroughly discussed.

In this work, the mechanisms of degraded mobility in narrower NWs are investigated by low temperature measurements. It is found the hole mobility in NW pFETs is severely degraded by surface roughness scattering in side surface channels while the effect of side surface roughness is limited in NW nFETs.

2. Experiment

Temperature dependence of carrier mobility in tri-gate single NW FETs (μ_{NW}) with [110] direction channel on (100) SOI wafers was measured with split C-V method from room temperature (RT) down to 6 K. The NW height H_{NW} is 12.5nm, and NW length L_{NW} is 53μm. The minimum NW width (W_{NW}) is 11nm. Detailed device structure and mobility extraction method is described in [7].

3. Results

Figs. 1 and 2 show measured μ_{NW} in single NW FETs at various temperatures. The increase in μ_{NW} as decreasing temperature is observed. Figs. 3 and 4 show temperature dependence of μ_{NW} with various W_{NW} at $N_{inv}=8\times10^{12}$ cm^{-2} for electrons and $N_{inv}=7\times10^{12}$ cm^{-2} for holes. It is clearly observed that measured μ_{NW} saturates at temperature below 20 K. At this high N_{inv}, effects of Coulomb scattering can be ignored. Since phonon scattering limited mobility (μ_{phonon}) can also be ignored at such low temperature, μ_{NW} at 6 K can be considered as the surface roughness scattering limited mobility (μ_{sr}). Fig. 5 and Fig. 6 show the width dependence of μ_{NW} at different temperatures. μ_{sr} degrades significantly as W_{NW} decreases, suggesting the surface roughness related scattering has more influence in the narrower NWs.

By using the Matthinessen's rule of $1/\mu_{phonon}=1/\mu_{NW}-1/\mu_{NW}(6K)$, μ_{phonon} in NW FETs is extracted. Figs. 7 and 8 show temperature dependence of μ_{phonon}. The phonon scattering in NWs has little width dependence and the slope of the double logarithmic scale is in good agreement with reported values of -1.75 in planar bulk FETs [8]. Therefore, it is confirmed that μ_{phonon} degradation is small in NWs, indicating that the mobility degradation in narrower NWs originates from the degradation of μ_{sr}.

μ_{NW} can be understood as the weighted average of mobility contribution from the three surfaces in tri-gate NW FETs [6],

$$\mu_{NW}=\mu_{top}\frac{W_{NW}}{W_{NW}+2H_{NW}}+\mu_{side}\frac{2H_{NW}}{W_{NW}+2H_{NW}}=(1-\alpha)\mu_{top}+\alpha\mu_{side}=\mu_{top}+\alpha(\mu_{side}-\mu_{top})$$

in which $\alpha=2H_{NW}/(W_{NW}+2H_{NW})$ is "side surface ratio", μ_{top} is top surface mobility and μ_{side} is side surface mobility. In [110]-NWs on (100) SOI, the top surface is (100) and side surfaces are (110).

Figs. 9 and 10 show α dependence of μ_{NW} at various temperatures. Since μ_{NW} at 6K corresponds to μ_{sr}, top surface μ_{sr} (α=0) and side surface μ_{sr} (α=1) are successfully derived from these figures. Apparently, μ_{sr} of (110) side surfaces are severely degraded in both electrons and holes, possibly due to process-induced roughness.

In Figs. 11 and 12, measured μ_{NW} as well as extracted μ_{sr} and μ_{phonon} are plotted against α at 300K. Here, the blue line is the "ideal" μ_{NW} at 300K, which is obtained using universal (100) and (110) mobility [9]. In NW nFETs, measured μ_{NW} is on the ideal μ_{NW} line. Although μ_{sr} of (110) side surfaces is degraded, electron mobility in the (110) side surface is originally low and the effect of degraded μ_{sr} is very small. It is confirmed that the decrease in μ_{NW} in narrower NW nFETs is simply caused by low electron mobility in side (110) surface.

In NW pFETs, on the other hand, measured μ_{NW} is much smaller than the ideal μ_{NW}, and extracted μ_{sr} and μ_{phonon} are comparable. Ideally, μ_{NW} should increase in narrower NW pFETs thanks to high hole mobility in side (110) surface. However, it is found that μ_{NW} in narrower NW pFETs is severely degraded because high mobility in side surfaces is seriously degraded by surface roughness. In order to take full advantage of high (110) hole mobility in NW pFETs, the improvements of side surface quality are mandatory.

4. Conclusions

Mobility degradation mechanisms in NW FETs are analyzed by low temperature mobility measurements. It is found that the side surface roughness is the main source of mobility degradation in NW pFETs.

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References

[1] T. Tezuka et al., IEDM, p.887, 2007. [2] S.D. Suk et al., IEDM, p.891, 2007. [3] N. Singh et al., IEEE EDL, VOL. 27, NO. 5, 2006. [4] J. Chen et al., VLSI, p.93, 2008. [5] J. Chen et al., IEDM, p.757, 2009. [6] J. Chen et al., VLSI'10, p.175. [7] K. Mao et al., to be presented in SSDM, 2012. [8] S. Takagi et al., IEEE TED, Vol. 41, p. 2357, 1994. [9] H. Irie et al., IEDM, p.225, 2004.

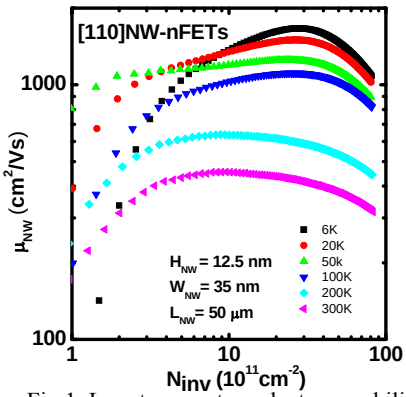

Fig.1. Low temperature electron mobility in [110] NW-nFETs.

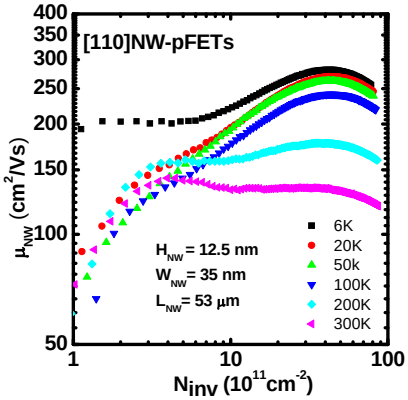

Fig.2. Low temperature hole mobility in [110] NW-pFETs.

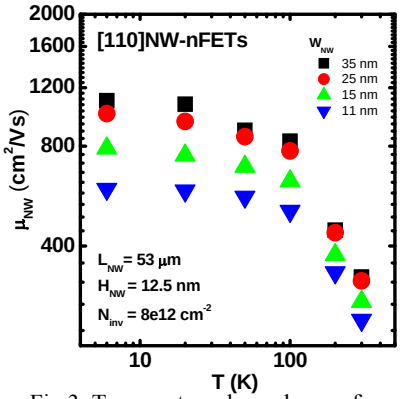

Fig.3. Temperature dependence of electron mobility in [110] NW-nFETs.

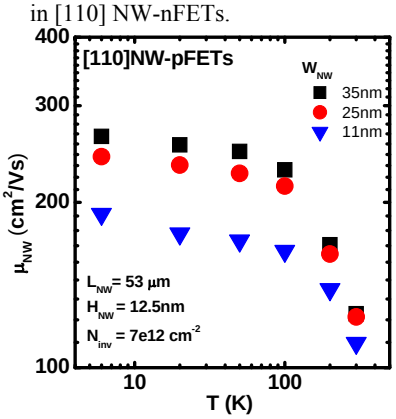

Fig.4. Temperature dependence of hole mobility in [110] NW-pFETs.

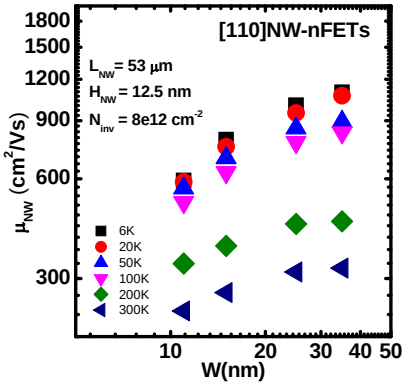

Fig.5. Width dependence of electron mobility in [110] NW-nFETs.

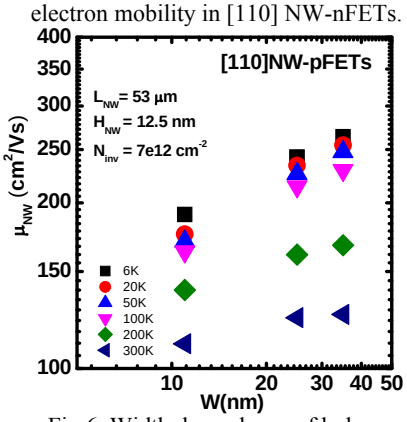

Fig.6. Width dependence of hole mobility in [110] NW-pFETs.

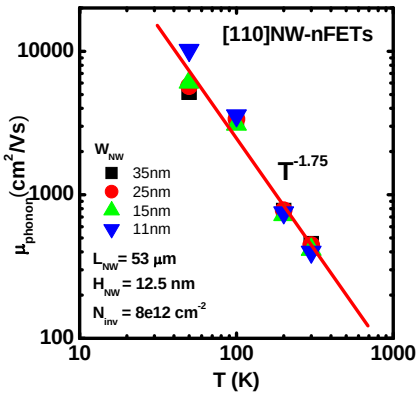

Fig.7. Temperature dependence of μ_{phonon} in [110] NW-nFETs.

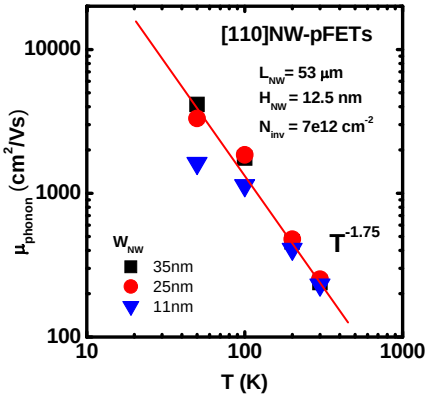

Fig.8. Temperature dependence of μ_{phonon} in [110] NW-pFETs.

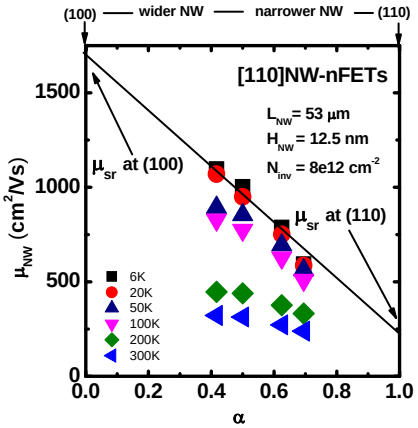

Fig.9. α dependence of electron mobility in [110] NW-nFETs.

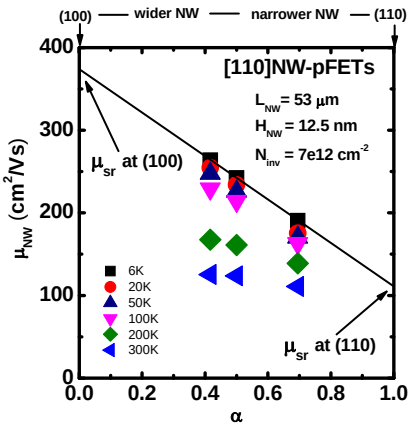

Fig.10. α dependence of hole mobility in [110] NW-pFETs.

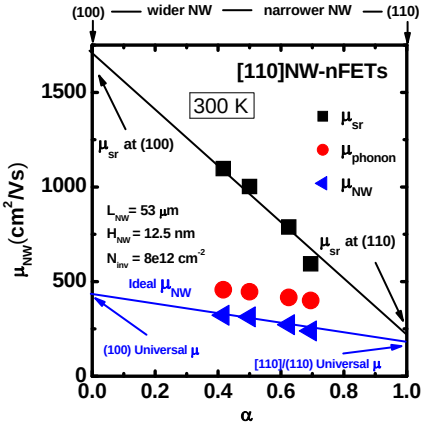

Fig.11. α dependence of electron mobility at RT in [110] NW-nFETs.

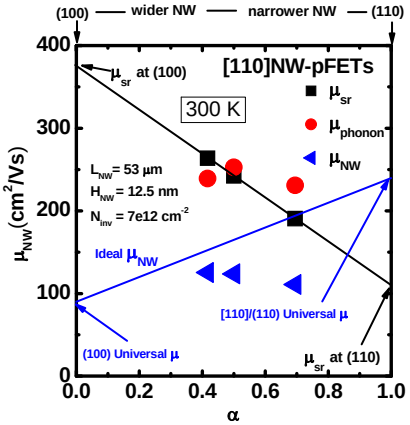

Fig.12. α dependence of hole mobility at RT in [110] NW-pFETs.