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III-V/Ge Channel MOS Transistor Technologies for Advanced CMOS

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1. Introduction MOSFETs using III-V/Ge channels with high mobility and low effective mass have been regarded as strongly important for obtaining high current drive and low supply voltage CMOS under sub 10 nm regime. One of the ultimate CMOS structures can be the combination of III-V nMOSFETs/Ge pMOSFETs (Fig. 1) [1]. Fig. 2 shows a variety of possible applications of III-V/Ge on the Si platform. In the More Moore approach, several CMOS configurations are possible. If high performance Ge nMOSFET or III-V pMOSFET are realized, Ge CMOS or III-V CMOS is also viable. Also, this heterogeneous integration is expected to create novel LSIs or SoC utilizing a variety of device families along the More-than-Moore and the Beyond-CMOS approaches.

However, there are still many technological issues to be solved for realizing Ge/III-V-based CMOS on Si substrates (Fig. 3), such as (1) high quality Ge/III-V film formation on Si substrates (2) gate insulator formation with superior MOS/MIS interface quality (3) low resistivity source/ drain (S/D) formation (4) total CMOS integration. In this paper, we present several viable solutions for the above critical issues for InGaA(InAs) and Ge MOSFETs. Also, we present an example of the integration of Ge and III-V MOSFETs on a same wafer through the combination of the developed technologies.

2. III-V MOS Technologies The high quality III-V channel formation on the Si platform is challenging. We are employing the direct wafer bonding of InGaAs/InP wafers with Si substrates for fabricating the InGaAs(InAs)-on-Insulator substrates mainly using ALD Al_2O_3 BOX [2-4], as typically shown in Fig. 4. We have fabricated extremely-thin 3.2-nm-thick InGaAs-OI substrates with 7.7-nm-BOX, resulting in the MOSFET operation with low leakage current. Fig. 5 shows TEM photos of $In_{0.3}Ga_{0.7}As$(3nm)/ InAs(3nm)/$In_{0.3}Ga_{0.7}As$(3nm)-OI MOSFETs on Si, confirming the high uniformity.

Low-resistance S/D formation is one of the critical issues for extremely-thin body devices. Here, metal S/D scheme can be the best solution for III-V nMOSFETs/Ge pMOSFETs from the viewpoint of Fermi level pinning positions of metals on III-V and Ge. Recently, we have found that a Ni-InGaAs alloy formed by direct reaction of Ni and InGaAs [4, 5], shown in Fig. 6, can realize self- aligned metal S/D structures for InGaAs MOSFETs. Ni-InGaAs alloy layers exhibited low sheet resistance of around 25 Ω/square, which is lower by 1/3 than that of InGaAs layers doped with n-type impurities up to the solid solubility (~80 Ω/square). Also, $In_xGa_{1-x}As$ with higher Indium content, x, can provide lower Schottky barrier height or ideally no barrier, as also shown in Fig. 6. We can confirm uniform Ni-InGaAs S/D formation in the extremely-thin InGaAs-OI structure and the encroachment toward the channel in Fig. 5. Fig. 7 shows the I_D-V_G characteristics of the InAs-OI MOSFET with L_{ch} of 55 nm and DIBL as a function of L_{ch} [4]. In spite of thick EOT of 3.5 nm (6 nm Al_2O_3), the device exhibits good transfer and output characteristics with small DIBL, owing to the extremely-thin channel thickness of 3 nm.

3. Ge MOS Technologies Ge MOSFETs would be regarded as more matured than III-V ones. Here, one of the most critical issues is the realization of gates stacks with superior MOS interfaces. Recent studies [6, 7] have revealed that Ge oxide interfacial layers (IL) can provide superior MOS interfaces. We have recently proposed and demonstrated a novel technology to form thin GeO_x IL by using post plasma oxidation after depositing ALD Al_2O_3 or HfO_2/Al_2O_3 on Ge [8-10], shown in Fig. 8. This plasma process significantly reduces D_{it} with minimal increase in EOT (Fig. 9). Thinner EOT and lower gate leakage current can be realized with maintaining low by under the HfO_2/Al_2O_3 gate stacks, where Al_2O_3 is necessary to block the inter-diffusion between Ge and HfO_2.

The I_d-V_d and I_d-V_g characteristics of a Ge pMOSFET with HfO_2(2.2nm)/Al_2O_3(0.2nm)/GeOx/Ge having EOT= 0.76 nm are shown in Fig. 11. A normal pMOSFET operation can be observed with an on/off ratio of ~10^4. We have obtained high hole mobility of 596 and 546 cm^2/Vs for EOT of 0.82 and 0.76 nm, respectively.

4. Integration of III-V/Ge MOSFETs In order to realize the integration of III-V/Ge MOSFETs, III-V substrates were bonded with Ge substrates. Fig. 12 shows the schematic view and TEM photos of a fabricated InGaAs-OI/Ge CMOS structure [11]. The Al_2O_3 gate stacks and Ni-based metal S/D were employed. Here, plasma post oxidation was applied to reduce D_{it} in Ge MOSFETs. The electron and hole mobility of 1800 and 260 cm^2/Vs and the mobility enhancement against Si of 3.5× and 2.3× have been demonstrated for InGaAs-OI nMOSFETs and Ge pMOSFETs (Fig. 13), respectively.

5. Conclusion A variety of viable MOS device/process technologies were addressed for solving the critical problems. The integration of InGaAs-OI nMOSFETs and Ge p-MOSFETs on a same wafer has been demonstrated.

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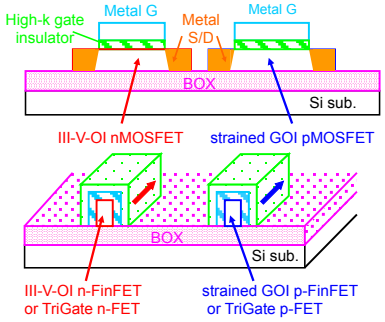

Fig 1 Ultimate CMOS composed of III-V nMOSFET and Ge pMOSFET.

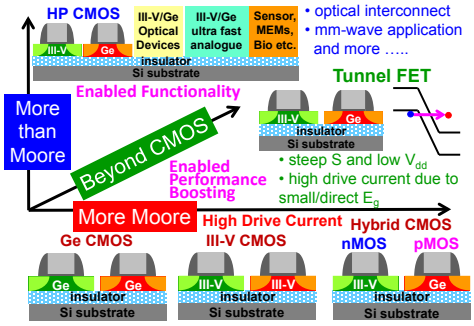

Fig.2 Possible evolution scenario for III-V/Ge devices on Si platform through heterogeneous integration.

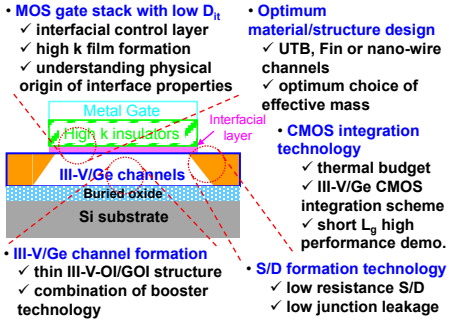

Fig.3 Critical issues for realizing III-V/Ge MOSFETs on the Si platform.

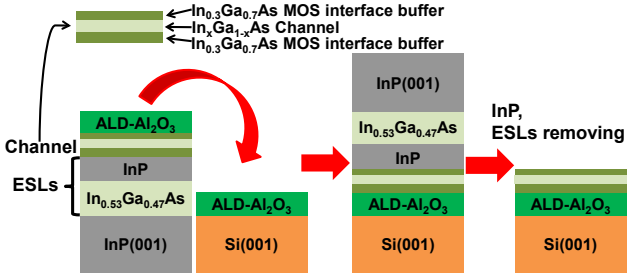

Fig.4 Formation of InGaAs channels with MOS interface buffers on Si by direct wafer bonding technique.

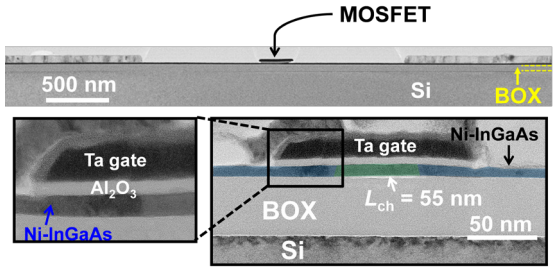

Fig.5 Cross-sectional TEM images of fabricated InAs-OI MOSFETs with L_{ch} of 55 nm with T_{body} of 3/3/3 nm.

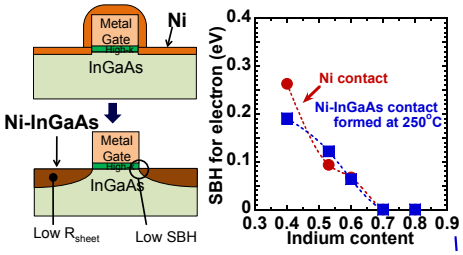

Fig.6 Fabrication process of self-aligned In-GaAs MOSFETs with Ni–InGaAs metal S/D and Schottky barrier height as a function of Indium content.

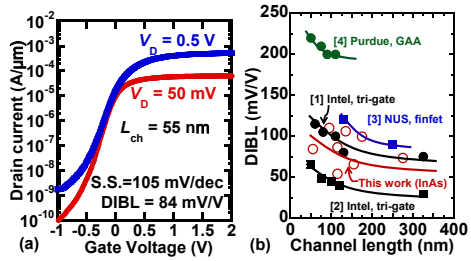

Fig.7 I_D-V_G characteristics of InAs-OI MOSFETs with T_{body} of 3/3/3 nm and T_{ox} = 6 nm and Benchmark of DIBL characteristics.

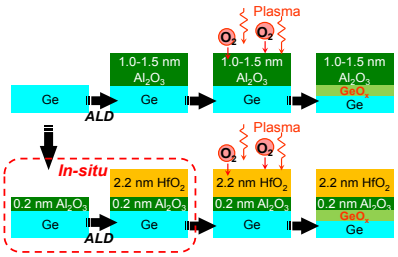

Fig.8 GeO_x/Ge interface formation by ECR oxygen post plasma oxidation through Al_2O_3 and HfO_2/Al_2O_3.

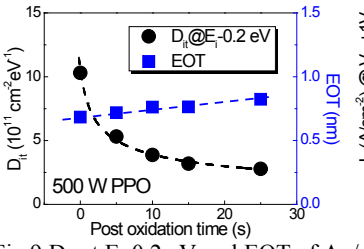

Fig.9 D_{it} at E_i-0.2 eV and EOT of Au/HfO_2(2.2 nm)/Al_2O_3(0.2 nm)/GeO_x/p-Ge MOS capacitors with different PPO times.

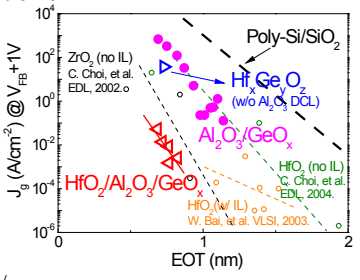

Fig.10 Gate leakage current of Au/Al_2O_3/GeO_x/n-Ge and Au/HfO_2/Al_2O_3/GeO_x/n-Ge MOS capacitors at V_{FB}+1 V.

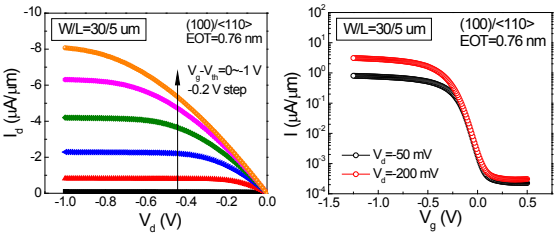

Fig.11 I_d-V_d of the Ge pMOSFET with $HfO_2/Al_2O_3/GeO_x$/Ge gate stack having 15 s' plasma post oxidation and I_d-V_g of the Ge pMOSFET with $HfO_2/Al_2O_3/GeO_x$/Ge gate stack having 15 s' plasma post oxidation.

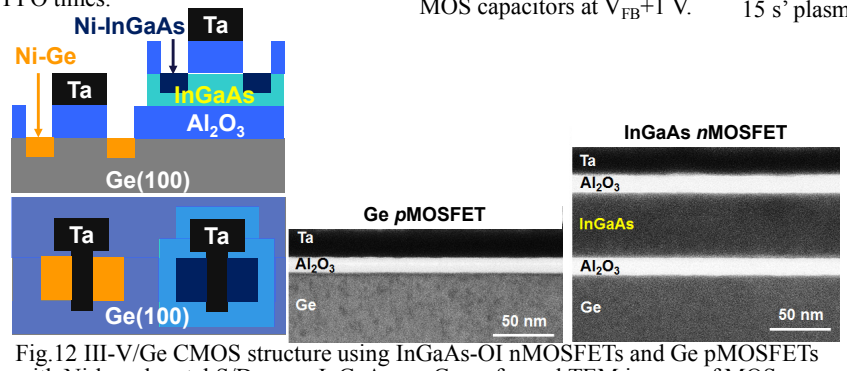

Fig.12 III-V/Ge CMOS structure using InGaAs-OI nMOSFETs and Ge pMOSFETs with Ni-based metal S/D on an InGaAs-on-Ge wafer and TEM images of MOS interfaces of InGaAs-OI nMOSFET and of Ge pMOSFET.

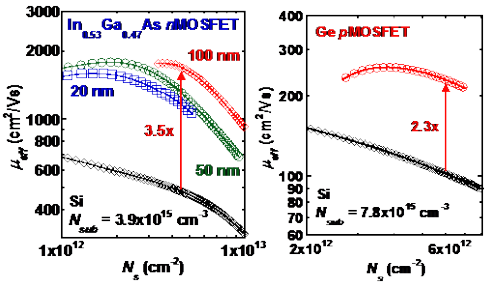

Fig.13 μ_{eff} – N_s characteristics of Ge pMOSFET and μ_{eff}–N_s characteristics of 20-, 50-, and 100-nm-thick InGaAs-OI nMOSFETs.