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A Physics-Based Compact Model of Tunnel-FETs Considering Nonlocal Effects

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1. Introduction

One of the urgent issues in developing tunnel-FETs (TFETs) is a compact model, because TFETs have some specific aspects to be considered in building circuits. Physics of TFETs is based on nonlocal band to band tunneling (BTBT) phenomena, which causes difficulties in compact modeling. In this paper, a new compact model of TFETs is proposed considering nonlocal aspects of BTBT. The model explains our measurements well including dependencies on physics based parameters. In addition, the model considers leakage currents, diode currents, Esaki tunneling, and capacitances. The model is described by Verilog, not as a table model but as a physics based analytical model, and thus ready to be used for practical circuit design.

2. Models

Nonlocal BTBT currents

While many device structures are proposed as TFETs, it is natural to choose a simple SOI TFET structure as a start of compact modeling. Origin of drain currents is nonlocal band to band tunneling occurred at source gate overlap region. To describe this nonlocal aspect, we introduce an assumption that each of tunnel paths consists of two parts, vertical path to the interface, and lateral path along the channel, as shown in fig.1. The vertical path could be easily determined by gate-insulator-source MOS approximation. A key part of the present model is estimation of the horizontal energy band profile. We formulate it by combining the gate-to-channel and the channel-to-source capacitances as compared to TCAD results in fig.2. Using these approximations, a tunnel distance is obtained which are equivalent for nonlocal electric field. This field is used in famous Kane's formula of BTBT generations.

Other effects in TFETs

In order to fully consider physics of TFETs, following effects should also be considered in the compact model.

A) Esaki tunneling and PN-diode currents are important in case of reversely biased source and drain.
B) Drain side BTBT is important for leakage analysis.
C) Temperature dependencies different from conventional CMOS.
D) Capacitances differ from MOSFETs because of the drain-channel connections.
E) Material effects to cover many candidates for TFETs.

All of these effects are newly implemented as physics based analytical formulations.

3. Results

Id-Vg characteristics calculated by the present model are shown in fig.3, compared with our measurements [2] and TCAD nonlocal-model simulations [1]. Main features of our TFETs are well explained by both TCAD and the present model, including leakage currents in *Vgs*>0. The discrepancies around *Vgs~0V* are effects of gate currents measured in our *EOT~1nm* device. Agreement to the device, and also to our advanced TCAD model [1] ensure the adequacy of our assumptions on the nonlocal aspects of BTBT effects explained in the previous section.

Id-Vd characteristics are shown in fig.4, compared with TCAD results. Esaki tunneling effects in reverse *Vds* conditions are successfully expressed as discussed in ref.[5].

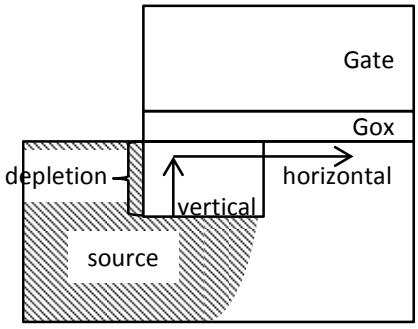

Fig.1 Schematic draw of the assumption of the present model. Each tunnel path consists of vertical and horizontal paths.

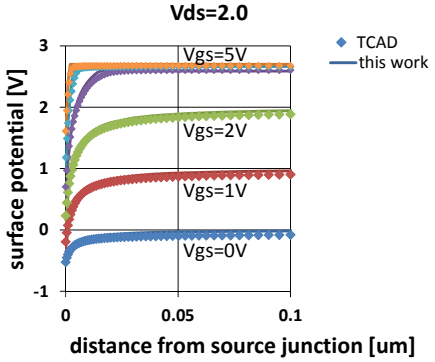

Fig.2 Assumed surface potential compared with TCAD.

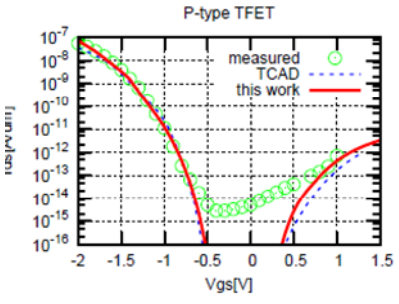

Fig.3 Id-Vg characteristics of a TFET. Measurements, TCAD, and the present model are compared.

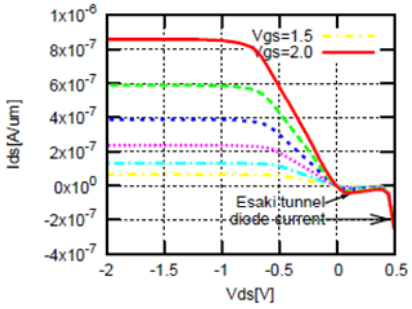

Fig.4 Id-Vd characteristics of a TFET calculated by the present model.

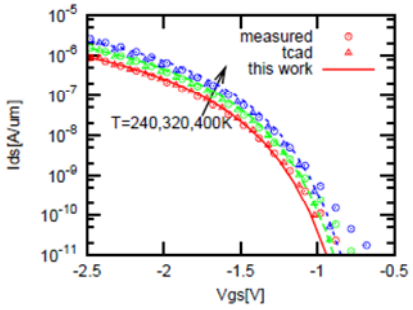

Fig.5 Temperature dependence of TFET, measured, TCAD, and this work are compared.

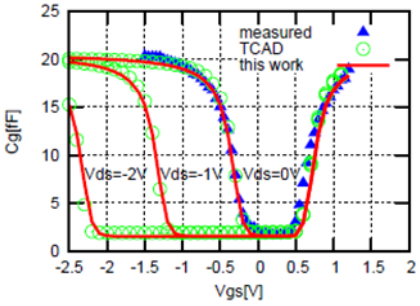

Fig.6 CV curves of P-type TFET, Measured (only Vds=0V), TCAD and the present model are compared.

Temperature dependences of Id-Vg characteristics are compared also to our measurements and TCAD simulations in fig.5. The temperature dependence model of BTBT generations in ref.[6] is used.

CV-curves are compared in fig.6, with measurements only for *Vd=Vs*, and with TCAD with *Vd*-dependencies. Gate capacitances are mainly connected to drain, because of the junction-less drain structures of TFETs.

4. Circuit Simulations

DC and transient simulations of a Si TFET inverter are shown in fig.7. In case of *nsec.*-scale, small drain currents results in large delay of the inverter, which result in large under- and overshoot of output voltages. In case of *usec.*-scale, such undesirable behaviors are not observed. Thus we can now discuss target applications corresponding to the device performances.

It is interesting to see how the material affects the circuit performances. The present model includes basic semiconductor parameters which can be used to investigate material effects. Fig.8 shows Ge 0.5V TFET inverter simulations, using parameters are taken from ref[6].

Fig.9 shows Ge 0.5V SRAM static noise margin simulation results. Transfer gates in SRAMs are one of the problems caused by drain-source asymmetry of TFETs. The present model enables discussions concerning such problems of circuit design using TFETs.

5. Conclusions

A physics-based TFET compact model is suggested, with nonlocal BTBT effects using approximation of surface potentials. Esaki effects, temperature dependences, material parameters, and capacitances are considered and successfully confirmed through comparisons to our measurements and TCAD with nonlocal BTBT models. The present model is ready for practical study of building circuits by TFET technologies.

Acknowledgements

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References

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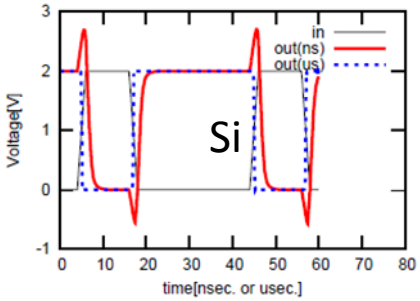

Fig.7 Si 2V TFET inverter simulation for nsec. and usec. conditions.

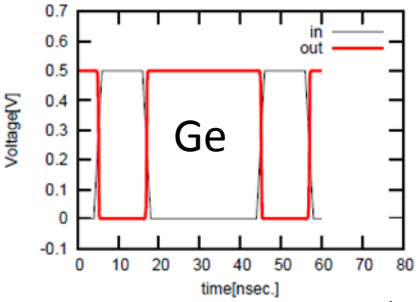

Fig.8 Ge 0.5V TFET inverter simulation.

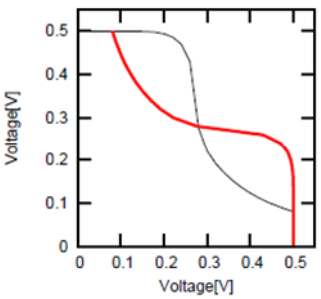

Fig.9 Butterfly curves of Ge 0.5V TFET SRAM.