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Tunnel Field Effect Transistor with Epitaxially Grown Steep Tunnel Junction Fabricated by Source/Drain-first and Tunnel-junction-last Processes

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1. Introduction

There is a strong demand to develop energy–efficient device technologies. Reducing the operation voltage of microchips to reduce their power consumption is an effective way to achieve this goal. However, the subthreshold swing (SS) of a metal–oxide–semiconductor field-effect transistor (MOSFET) is limited to 60 mV/decade; it is governed by the operation mechanism. This makes it difficult to greatly reduce the MOSFET operating voltage. To achieve this, novel devices with different operation mechanisms are required. Tunnel FETs (TFETs) are promising for such steep-SS devices. They utilize band-to-band tunneling (BTBT) of semiconductors. [1-6] Several research groups have demonstrated sub-60 mV/decade SS TFETs.

In TFET fabrication, it is essential to form an abrupt dopant profile in the source tunnel junction since this enhances the tunneling probability, which generates sufficiently high BTBT transport. In the present study, we used epitaxial growth to realize a steep dopant profile. [3] We fabricated a Si TFET with an epitaxially grown steep tunnel junction by a novel tunnel-junction-last process combined with a source/drain-first process. Using this improved FET process, p- and n-TFETs and their electrical properties were studied.

2. Experimental

Figs. 1(a) and (b) respectively show schematic diagrams of the device structures of conventional and modified TFETs fabricated on silicon-on-insulator (SOI) wafers. The modified TFET has an epitaxially grown channel layer (epi-ch.) between the source and gate layers. The epi-channel layer overlaps with the source and gate regions (L_{OV} indicates the overlap length in Fig. 1). **Fig. 2** shows the operation mechanism of the epi-channel TFET. The Si epi-channel acts as a parallel-plate capacitor. The applied gate potential initiates BTBT transport parallel to the gate electric field. [**Fig. 2(b)**] The parallel-plate capacitor has a larger tunneling area than a conventional TFET, which increases the drain current. [**Fig. 2(c)**] [3,7-9] **Fig. 3** shows the schematic process flow of epi-channel p- and n-TFETs. The process is based on a source/drain-first FET process. For a III–V TFET, it is essential to tune the energy-band alignment to maximize BTBT transport by tuning the composition of the III–V materials. This means that different source (substrate) compositions are required for p- and n-TFETs for complimentary MOS (CMOS) applications. However, in the present study, both p- and n-TFETs are fabricated on a single SOI wafer without intentional doping. The source and drain regions are preferentially created by BF_2 or P implantation and activation annealing is then performed at 1000 °C. To suppress the off-current of the TFET, we form gradual source or drain junctions on SOI wafers by post-implantation annealing. An undoped thin Si channel is epitaxially grown on source/drain-first SOI wafers by the tunnel-junction-last process. After OH termination of the epitaxial Si layer, a 3–5-nm-thick HfO_2/Al_2O_3 high-*k* gate insulator and a 40-nm TiN gate electrode are deposited by atomic layer deposition and sputtering. After gate patterning, contact formation, and H_2 sintering, the electrical properties were measured.

3. Results and discussion

Fig. 4 shows cross-sectional transmission electron microscopy (X-TEM) images of the epi-channel TFET and a TiN/high-*k*/epi-channel/SOI stack. They reveal that a thin epitaxial layer containing few defects was produced. The dopant depth profiles in the epi-channel/source stacks were measured by front-side secondary ion mass spectroscopy (SIMS) analysis (**Fig. 5**). A very steep (~1.5 nm/decade) doping profile was realized. **Fig. 6** shows the I_D–V_{GS} characteristics of p- and n-TFETs with epi-channels. The p- and n-TFETs exhibited symmetric on/off operation. **Fig. 7** compares I_D of conventional and epi-channel TFETs. The epi-channel TFET shows better SS and I_D values than the conventional one, even with larger equivalent oxide thickness (EOT).

Fig. 8 shows the I_D variation against the overlap length. A larger L_{OV} increases the tunneling area (see **Fig. 2**). I_D increases with increasing L_{OV} and I_D has a maximum at $L_{OV} \approx 50$ nm. For $L_{OV} > 50$ nm, I_D decreases with increasing L_{OV} (see inset in Fig. 8). **Fig. 9** shows the gate leakage current (J_G) variation against L_{OV}. J_G increases linearly with increasing L_{OV}. This implies that a large gate leakage current directly degrades the tunneling current and that an excessively high L_{OV} suppresses the drain current. To realize a larger I_D in an epi-channel TFET, it is essential to suppress the gate leakage current and reduce the resistivity of the thin channel layer.

4. Conclusion

We demonstrated Si TFETs with an epitaxially grown steep tunnel junction. A parallel-plate tunneling mechanism with a thin epitaxial Si channel is combined with p- and n-TFETs by a CMOS-compatible junction-last process. The overlap length can be tuned to increase the drain current. However, increasing the gate leakage current by increasing the overlap length too much severely degrades the drain current.

Acknowledgements

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References
[1] W.Y. Choi, et al., Electron Device Letters 28 (2007) 743.
[2] S.-H. Kim, et al., Symp. VLSI Tech. Dig. (2009) 178.
[3] R. Li, et al., physica status solidi C (2011) 1.
[4] T. Mori, et al., Jpn. J. Appl. Phys. 50 (2011) 06GF14.
[5] S. Salahuddin, and S. Datta, Nano Letters 8 (2008) 405.
[6] K. Jeon, et al., Symp. VLSI Tech. Dig. (2010) 121.
[7] C. Hu, et al., VLSI-TSA 2008 (2008) 14.
[8] R. Asra, et al., Jpn. J. Appl. Phys. 49 (2010) 120203.
[9] R. Asra, et al., IEEE Trans. Electron Devices 58 (2011) 1855.

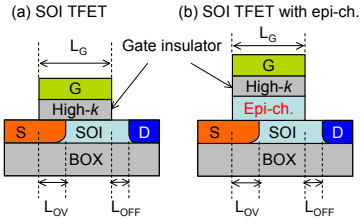

Fig. 1 Schematic models of (a) conventional SOI TFET and (b) SOI TFET with epi-channel used in the present study. The overlap length (L_{OV}) between the drain and gate regions in the device structure is shown. The physical gate length (L_G) and the drain offset length (L_{OFF}) are also indicated.

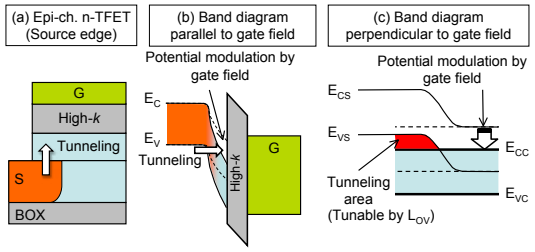

Fig. 2 Schematic diagrams of operation mechanism of epi-channel TFET. In (b) E_C and E_V indicate conduction and valence bands of the source Si, respectively. In (c), E_{CS} and E_{CC} indicate conduction bands in the source and the channel, respectively.

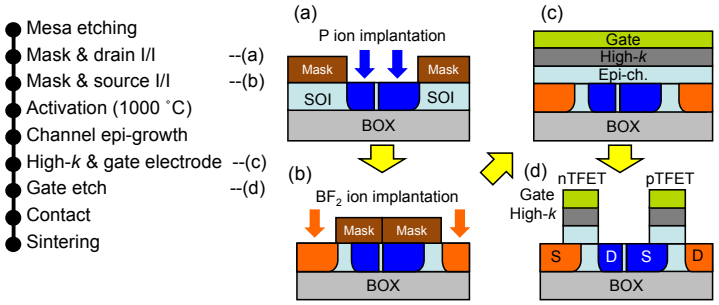

Fig. 3 Schematic process flow of p- and n-TFETs with an epi-channel by novel junction-last processes.

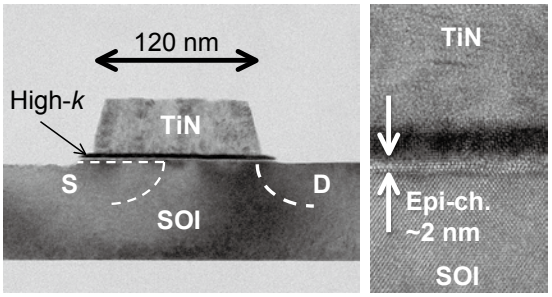

Fig. 4 Typical X-TEM images of (a) epi-channel TFET and (b) magnified TiN/high-k/epi-channel/SOI stack. Dashed lines indicate preferentially implanted source and drain regions.

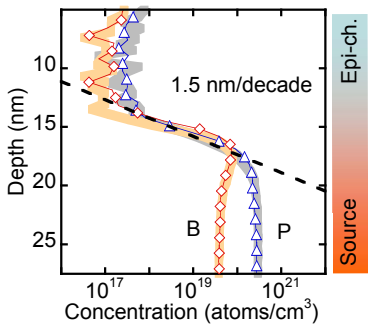

Fig. 5 SIMS of epi-channel/source wells showing P and B profiles. Open symbols indicate dopant concentrations after additional annealing at 700°C for 60 s. They show no significant difference from profiles obtained after post-implantation annealing (thick solid lines).

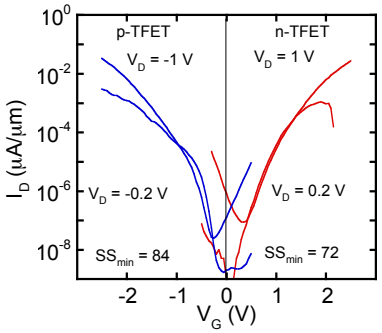

Fig. 6 Typical I_D–V_{GS} characteristics of p- and n-TFETs with an epi-channel. The EOT value of the high-k gate insulator is 1.3 nm.

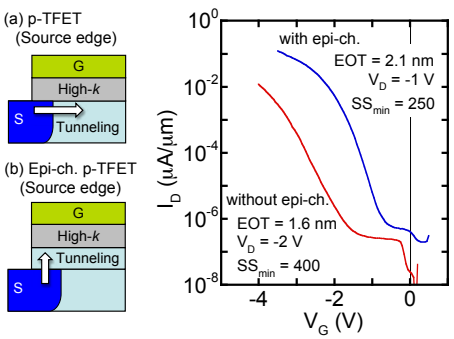

Fig. 7 Comparison of I_D characteristics of conventional and epi-channel TFETs.

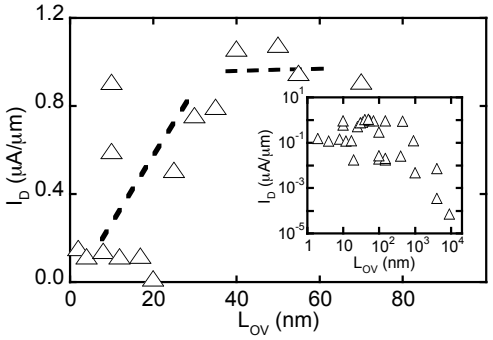

Fig. 8 I_D versus L_{OV} for epi-channel p-TFET. Inset shows log–log plot of I_D variation.

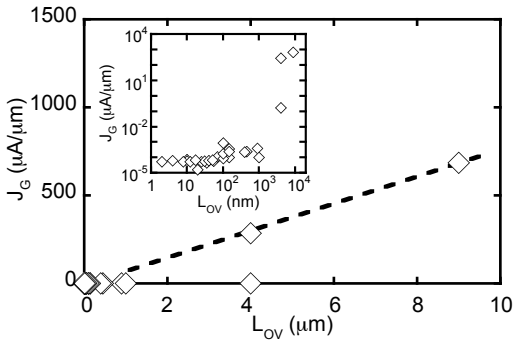

Fig. 9 J_G versus L_{OV} for epi-channel p-TFET. Inset shows log–log plot of J_G variation.