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First Demonstration of Tunnel Field-Effect Transistor Using InGaAs/Si Junction

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1. Introduction

Silicon very-large scale integration circuits (Si VLSIs) confront with huge power dissipation owing to increment of transistor integration because transistor scaling has inherent limitations such as enhanced OFF-state leakage current and short channel effect. A field-effect transistor (FET) with a lower leakage current and subthreshold slope (SS) is required for reducing the power dissipation because operation power is proportional to the square of the supply voltage. In order to reduce the supply voltage, reduction of off-state leakage current and the SS in a transistor are effective approach. Using a tri-gate and surrounding-gate structure has been proposed as an approach of reducing these parameters. Furthermore, III-V materials are expected as an alternative channel for future FETs. However, FETs have a physical limit in the SS owing to carrier diffusion mechanism (SS = 2.3 k_BT/q ~ 60 mV). Further scaling of power dissipation will be saturated because of this physical limitation.

Steep-slope transistors such as tunnel FETs (TFETs) [1-6] and impact ionization FETs [7] have therefore been investigated to overcome the physical limitation in SS. Among steep-slope transistors, the TFETs are promising transistor to achieve steep-slope SS with low power because carrier tunneling occurs under low electrical field. The use of the TFET with an SS of 10 mV/dec with keeping device performance as conventional FETs would reduce the required supply voltage to as low as 0.25 V, compared with the 0.9 – 1.0 V needs by a conventional FETs.

Recent progress in selective-area growth have enabled the integration of III-V nanowries (NWs) on Si regardless of mismatches in terms of lattice constant, thermal expansion coefficient, and polarity. And it has achieved a TFET using InAs NW/Si heterojunction [6]. However, misfit dislocations were found to degrade the device performance. Thus a heteroepitaxial system with lower lattice mismatch compared to InAs/Si is required for improving performance. Here, we investigate electrical properties in InGaAs NW/Si heterojunction and demonstrate TFET using InGaAs NW/Si with surrounding-gate architecture.

2. Experimental details

2-1. Growth of InGaAs NWs on Si by SA-MOVPE

The substrate was *p*-Si ($p \sim 1 \times 10^{18}$cm^{-3}) and p^+-type ($p \sim 2 \times 10^{19}$cm^{-3}) Si(111). After 20 nm-thick SiO_2 was formed by thermal oxidation, openings were formed using electron beam (EB) lithography and wet etching. InGaAs NWs were grown in low-pressure horizontal MOVPE system. Trimethylgallium (TMGa), trimethylindium (TMIn), and arsine (AsH_3) were used for growth materials. The partial pressures of TMGa, TMIn and AsH_3 were [TMGa] = 5.7×10^{-7} atm, [TMIn] = 9.2×10^{-7} atm, and [AsH_3] = 5.0×10^{-4} atm, respectively. Monosilane (SiH_4) was used for n-type dopant. The ratio of [TMIn]/{[TMIn] + [TMGa]} in vapor phase was 0.61. The growth temperature was 670°C and growth time was 10 min. Before the InGaAs NW growth, Si(111) substrate was annealed at 925°C in H_2 and treated in AsH_3 gas to form Si(111) 1×1:As surface [10]. At last, flow-rate modulation epitaxy (FME) was introduced to completely aligned the vertical InGaAs NWs on Si(111) as shown in Fig. 1(a). Fig. 1(b) shows the typical growth results of the InGaAs NWs on Si(111) substrate. The uniformed and vertically aligned InGaAs NWs were grown on Si(111). The average diameter of the InGaAs NWs was 80 nm, and the average height was about 1 μm. EDX line scan profile showed the In composition of the InGaAs NW was 70 ± 2% [10].

2-2. Fabrication process for FET structure.

A two terminal device was then fabricated by first

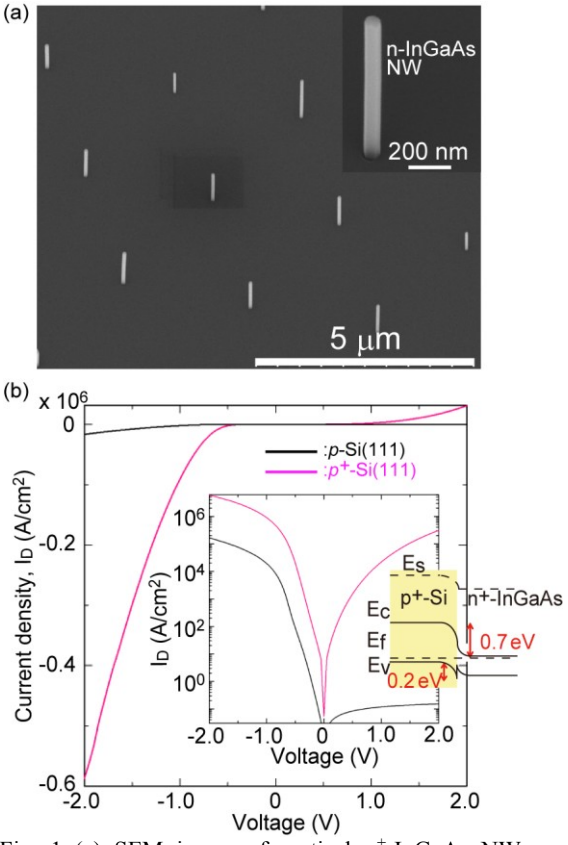

Fig. 1 (a) SEM image of vertical n^+-InGaAs NWs on p^+-Si(111) substrate. (b) Current-voltage characteristic of the NWs. The p^+-Si was grounded. Inset shows semi-log plot of the I-V curve and band diagram of the junction.

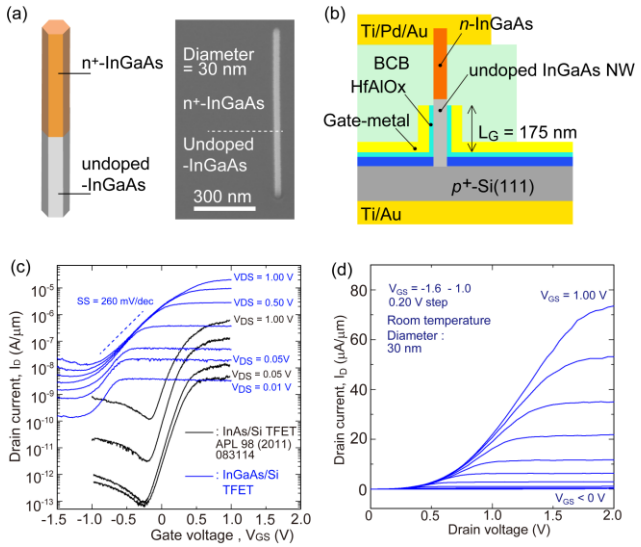

Fig. 2 (a) Schematic of the n^+-InGaAs/undoped InGaAs axial NW. SEM image of the growth result. The diameter of the NW is 30 nm. (b) Illustration of TFET structure. (c) Transfer characteristic of the TFET using InGaAs NW/Si junction (blue curves). Black curves are the data of TFET using InAs NW/Si heterojunction. (d) Output characteristic of the TFET using InGaAs NW/Si heteroiunction.

coating the NWs with benzocycrobutene (BCB, DOW CHEMICAL) by spin-coating. Then, 500 nm length of InAs were revealed by reactive-ion etching (RIE) of the BCB layer using O_2/CF_4 mixed gas.

Next, 100 nm thick Au/10 nm-thick Pd/10 nm thick Ti was evaporated to serve as top electrode of the NWs and on the backside of the Si substrate. The I-V curve (with the p^+-Si substrate grounded) is shown in Fig. 1(b). The current was normalized using number of NWs and diameter. Typical rectification was observed under negative bias (forward direction in this case). The ideality factor was approximately 1.9. Interestingly, the current under reverse direction (positive bias) for the InGaAs NW on p^+-Si was higher than the case of p-Si. This current is thought to be a Zener tunneling across the heterojunction and indicates tunneling probability across the InGaAs NW/p^+-Si became higher.

Next, we fabricated a TFET. A single vertically aligned n^+-InGaAs/undoped-InGaAs axial NW was grown on a p^+-Si substrate that has lithographically defined mask opening-area inside a 50 × 50 μm square SiO_2 mask. The device processes for the TFET were the same as previously reported [6]. First, atomic layer deposition was used to cover the surface of the NW with 20-nm-thick $Hf_{0.8}Al_{0.2}O_x$ for high-k gate dielectric. The oxide was annealed at 270°C in nitrogen (N_2) after this deposition. Next, photolithography-defined tungsten (W) gate-metal was deposited by RF sputtering. BCB was then spin-coated on the NW. Subsequently, the BCB and the W were etched by RIE at the same time. Next, the top part of the 1200 nm-long NW was revealed. Next, the device was spin-coated again with BCB for electrical separation between the gate-metal and drain-metal. The L_g was 200 nm, which corresponds to the length of the undoped InGaAs region. After the RIE, 20 nm of Ti, 10 nm of Pd and 100 nm of Au were evaporated to create drain and source electrodes.

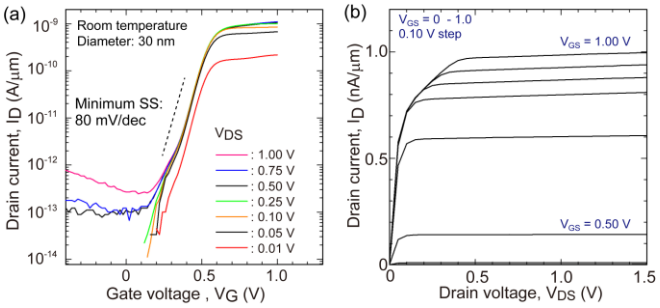

Fig. 3 (a) Transfer characteristic of the TFET using InGaAs NW (Si-doped InGaAs/Zn-compensated InGaAs axial NW)/ Si heterojunction. The SS was 80 mV/dec. (b) Output characteristic.

3. Results

Figure 2(b) shows typical transfer characteristic of the fabricated InGaAs NW/Si TFET at drain-source voltage (V_{ds}) of 0.05 – 1.00 V. In this case, the NW diameter was 30 nm shown in Fig. 2(a). The curve was measured using parameter analyzer (Agilent 4156C) at room temperature in the dark. The gate voltage (V_G) ranged from -1.00 to +1.00 V. The current values were normalized using outer perimeter of gate. Switching behavior with a SS of 260 mV/dec was observed under reverse bias direction (V_g is positive for n-p junction). This switching characterization appeared at the V_{DS} of 0.05 V. Also, the SS became slightly steeper with increasing the V_{DS}. The ratio of the ON/OFF current was approximately ~ 10^3 at V_{DS} of 1.00V. The ON- and OFF-state currents were about 2×10^{-5} A/μm, 2×10^{-8} A/μm respectively. The threshold voltage, V_{th}, of the I_D was -0.70 V. The output characteristic shown in Fig. 4(b) exhibits I_D had saturation region with increasing V_{DS}. Although the switching behaviors of the TFET were based on Zener tunnel transport across the III-V/Si heterojunction, the SS showed a large value. Since the SS of TFET is expressed as a function of V_G owing to Zener tunnel current [3], optimization of series resistances in TFET structure is important for biasing the V_{DS} effectively to tunnel junction, which results in small V_G operation, that is, steep slope switching. Thus, we at first investigated a doping effect for undoped InGaAs NW. Since the undoped InGaAs has unintentional (carbon) n-type doping under high V/III ration. The use of Zn doping for the undoped InGaAs NW growth can form intrinsic conductance with compensation effect. After the formation of Si-doped InGaAs/Zn-compensated InGaAs axial NW, TFETs using the axial NW with heterojunction shows sharp SS in transfer characteristic. In Fig. 3(a), switching behavior with a SS of 80 mV/dec was observed under reverse low bias direction. Also, the SS became slightly steeper with increasing the V_{DS}. T he ratio of the ON/OFF current was approximately ~ 10^5 at V_{DS} of 0.10V. Further improvements are required for attaining higher ON current and steeper SS.

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