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Sub-10-nm nano-sheet channel of Junctionless Poly-Si TFT with oxidation thinning method

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Abstract

A juncitonless (JL) poly-Si thin-film transistor (TFT) with sub-10 nm channel using oxidation thinning method. The sub-10 nm nano-sheet channel of single crystal-like is presented to obtain the excellent performance. The temperature dependence of parameters including ON-sate current and field effective mobility is analyzed in detail. Using NH_3 plasma treatment further improves the mobility, I_{ON}/I_{OFF}, and sub-threthold swing. The proposed JL TFT is promising for system on panel and high-density 3D stacked applications.

Introduction

The poly-Si TFTs have received a considerable attention in vertical stacking to increase device density [1]. Recently, junctionless (JL) MOSFET devices have been proposed for future nano-device application [2], [3]. Such a feature has also been demonstrated with poly-Si TFTs [4], [5]. The JL TFT transfer characteristics such as ON-state current and effective mobility are dominated by the thickness itself and the grain size of channel. The thickness of channel demands thinness to obtain the low OFF-state current. The adoption of large grain size as the channel has demonstrated superior performance, which exhibits the steeper sub-threshold swing (SS), high ON-state current, and large field effective mobility [6]. However, in the previously reports [4], [5], directly depositing the thin-film as the poly-Si channel in JL-TFTs may obtain the small grain size (see Fig. 1) suffered from the performance degradation mentioned above. Hence, this study investigates the poly-Si channel of JL TFTs utilizing oxidation thinning method to obtain the excellent performance.

Device Fabrication

The nano-sheet channel of JL-TFT was fabricated by initially growing a 400 nm-thick thermal silicon dioxide layer on 6 inch silicon wafers. A 40 nm-thick undoped amorphous silicon (a-Si) layer was deposited by low-pressure chemical vapor deposition at 550 ^oC. Next, the a-Si layer was solid-phase recrystallized (SPC) at 600 ^oC for 24 hours in nitrogen ambient. The SPC layer was implanted with 16-keV phosphorous ions at a dose of 1 × 1014 cm−2, followed by furnace annealing at 600 ^oC for 4 hours. The active layers, serving as ultra-thin channel, were defined by e-beam lithography and then mesa-etched by time-controlled wet etching of the buried oxide to form the omega-like shape on the edge of channel. Then, a 22-nm-thick dry oxide layer was grown as the sacrificial oxide layer and then dipped in dilute HF solution. Subsequently, an 8-nm-thick dry oxide was deposited as the gate oxide layer. Next, 250-nm-thick in-situ doped n+ poly-silicon was deposited as a gate electrode, and patterned by e-beam and reactive ion etching. A 200 nm-thick SiO_2 passivation layer was deposited. Finally, a 300 nm-thick Al-Si-Cu metallization was performed and sintered. For further improving the devices' performance, part of devices is passivated by NH_3 plasma treatment.

Result and Discussion

A schematic of grain boundary size processing is shown in Fig. 1. Fig. 2 depicts schematically view of JL-TFT and cross-transmission electron microscopic (TEM) photograph of sub-10 nm nano-sheet channel. A single crystalline-like cross-sectional view is observed in the poly-Si channel, shown in Fig. 2c. Fig. 3 represents transfer I_d–V_g and g_m–V_g characteristics of JL-TFTs. The I_{ON}/I_{OFF} current ratio exceeds 10^6. JL-TFT is a normally-on device with a threshold voltage (Vth) of –0.73 V, defined at $I_D = 10^{-8}$ A and $V_{DS} = 0.5$ V. Compared with the process of depositing thin-film layer directly as poly-Si channel [4], [5], using oxidation thinning process to form the sub-10 nm nano-sheet poly-Si channel with larger grain size exhibits a low subthreshold swing (SS) of 140 mV/dec at Vd = 0.5 V. Fig. 4 shows output characteristics of JL-TFTs. The I_{ON} is determined mainly by doping concentration of channel and appropriately proportional to the V_g. Fig. 5 shows simulated electron concentration profiles of JL and inversion-mode (IM) nano-sheet channel devices. JL devices will not suffer from serious surface scattering as the gate oxide is thinning, indicating that JL devices inherits the scaling advantages. Fig. 6 shows the I_d–V_g characteristics of JL-TFTs as a function of temperature. The inset of Fig. 6 exhibits the effective mobility extracted at the peak of transconductance and I_{ON} at $V_g - V_{th} = 3$ V as a function of temperature. The carrier mobility of JL-TFTs is mainly affected by impurity scattering varying as $T^{3/2}$, phonon scattering varying as $T^{-3/2}$, and potential barriers (V_B) scattering at the grain boundaries varying as exp ($-qV_B/kT$). The mobility is limited by grain boundaries and impurity scattering between 25 ^oC and 150 ^oC, while the mobility is limited by phonon scattering after 150 ^oC. Fig. 7 plots the I_d–V_g curves of the JL-TFTs with and without NH_3 plasma treatment. The inset table displays important parameters. The grain boundary defects density (N_t) can be extracted form the Id–Vg curves [7]. The NH_3 plasma-passivated device has larger field effect mobility, higher I_{ON}/I_{OFF} ratio, lower SS, and the lower N_t than the device without plasma treatment. It is worthwhile noting that the N_t is nearly the same before and after plasma treatment due to crystal-like channel. Table I shows a comparison of several key parameters in this work and other research.

Conclusion

This study demonstrates the fabrication and characterization of JL poly-Si TFTs of sub-10 nm channel using oxidation thinning process. The single crystal-like channel in the nano-sheet layer is obtained from the TEM and NH_3 treatment. The temperature dependence of parameters such as threshold voltage, ION, field effective mobility is analyzed. NH_3 plasma treatment improves the mobility, I_{ON}/I_{OFF}, and SS. This investigation explores its potential in future TFT for a system on panel and high-density 3D stacked applications.

Reference

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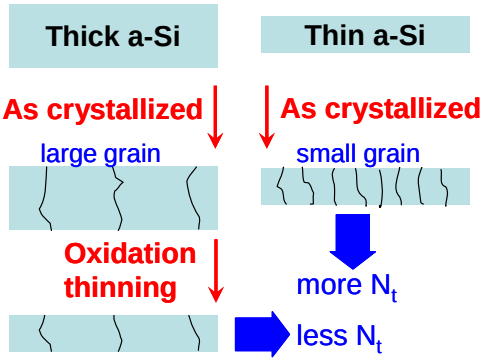

Fig. 1 Schematic of process flow for forming different grain boundary trap density (N_t)

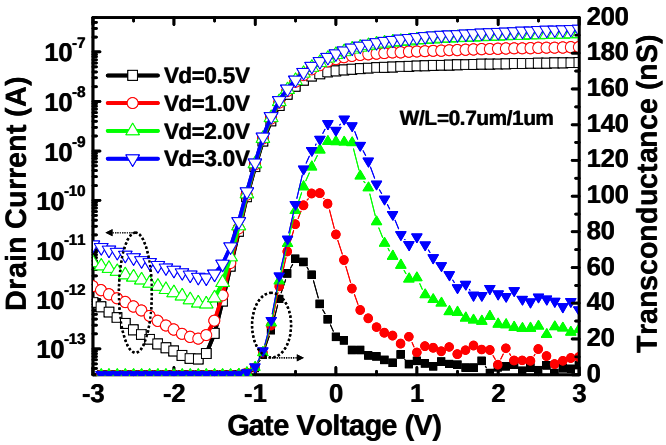

Fig. 3 Transfer characteristics I_d–V_g and g_m–Vg of JL-TFT with L = 1 μm and W = 0.7μm.

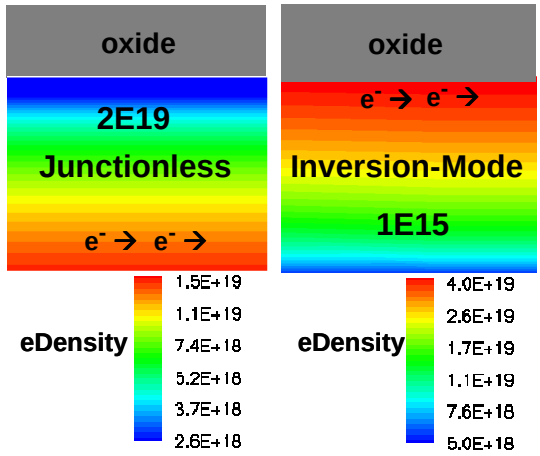

Fig. 5 Simulated electron density of JL and IM devices.

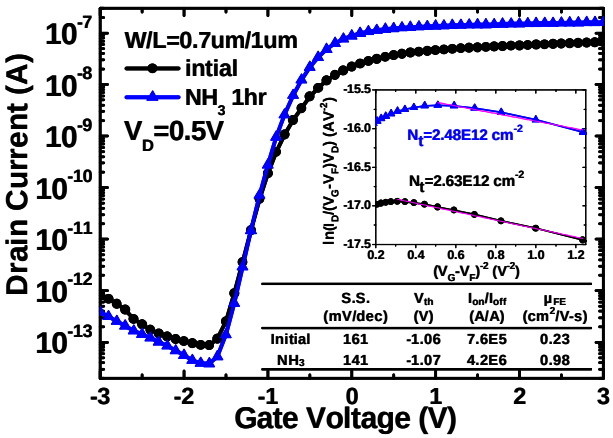

Fig. 7 Transfer curves of with and without NH_3 plasma. The N_t are extracted from the I_d–V_g curves in the inset.

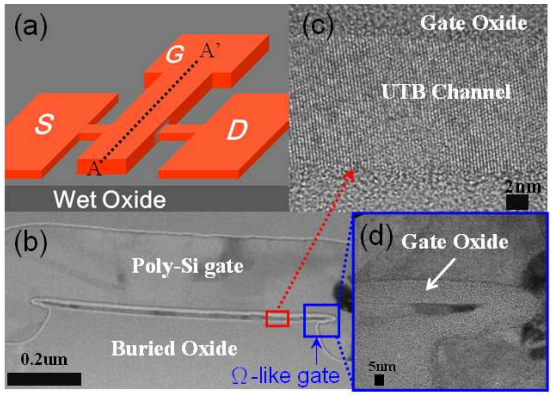

Fig. 2 (a) Schematic view of the JL-TFT and (b)–(d) the TEM micro-photograph of devices. A single crystalline view is observed.

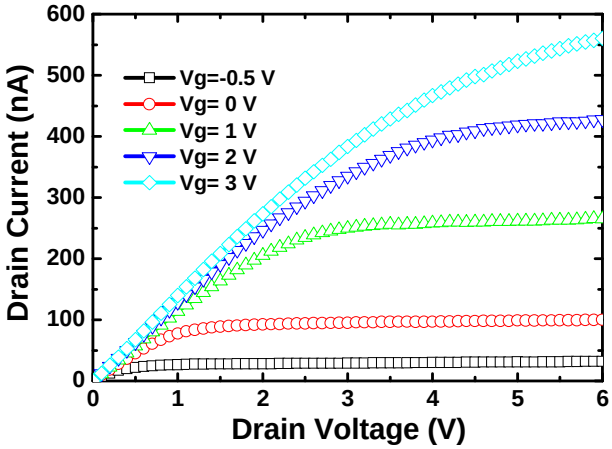

Fig. 4 Output characteristics I_d–V_d of JL-TFT.

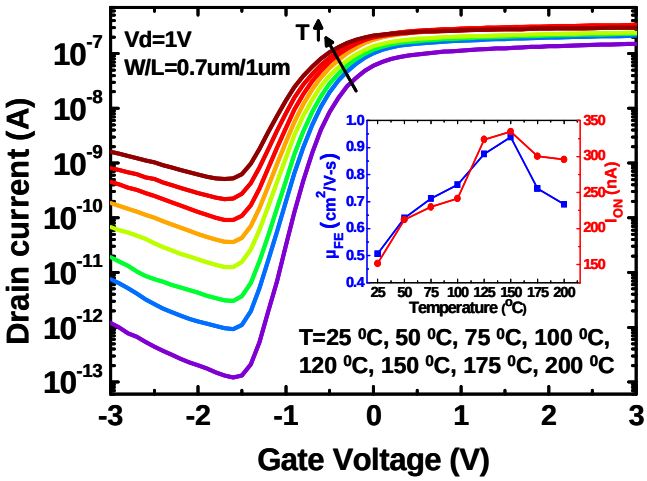

Fig. 6 I_d–V_g characteristics with various temperature of JL TFTs. The Inset shows the mobility and ON-state current of JL TFTs as a function of temperature.

	This work	Ref. A [4]	Ref. B [5]
Cross-section	**Flat Rectangular**	Rough Rectangular	Flat Rectangular
Channel structure	**N-SPC JL-planar**	N-SPC JL-GAA	N-SPC JL-Planar
NH_3 Plasma	**W/1hrs**	W/O	W/O
W /L (μm/μm)	**0.7/1**	0.07x2/1	10/5
Channel thickness (nm)	**10**	12	10
EOT (nm)	**8**	15	8
S.S. (mV/ dec.)	**141**	199	240
I_{ON}/I_{OFF} (V_G:V_D)	**$>10^6$ (3V;0.5V)**	$>10^6$ (5V;1V)	$>10^7$ (3V;0.1V)

Table I Comparison of important parameters from this works to other published results in JL-TFTs.