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Experimental Observation of Record-high Electron Mobility of Greater than 1100 $cm^2V^{-1}s^{-1}$ in Unstressed Si MOSFETs and Its Physical Mechanisms

Teruyuki Ohashi[1,3], Tsunaki Takahashi[1,3], Tetsuo Kodera[2], Shunri Oda[2], and Ken Uchida [1,3]
[1]Dept. of Physical Electronics & [2]Quantum Nanoelectronics Research Center, Tokyo Institute of Technology
2-12-1-S9-11, Ookayama, Meguro, Tokyo, 152-8552, Japan
[3]Dept. of Electrical and Electronics Engineering, Keio University
3-14-1 Hiyoshi, Kohoku, Yokohama, Kanagawa 223-8522, Japan
*Phone/Fax: +81-3-5734-2542 , E-mail: teruyuki.ohashi@ssn.pe.titech.ac.jp, uchidak@elec.keio.ac.jp

1. Introduction

Electron mobility (μ_e) of bulk Si with low doping concentration is reported to be approximately 1500 $cm^2V^{-1}s^{-1}$ [1]. However, it is well known that μ_e of bulk unstressed Si MOSFETs with extremely low substrate impurity concentration (universal mobility) never exceeds 1000 $cm^2V^{-1}s^{-1}$ [2], even when MOSFETs are fabricated in perfectly controlled manufacturing facilities. Although one might consider that interface states (N_{it}) could be the origin of the lower μ_e, N_{it} is too low to explain the observed μ_e degradation. Therefore, much worse μ_e of Si MOSFETs has been a big mystery.

In this study, μ_e of greater than 1000 $cm^2V^{-1}s^{-1}$ is demonstrated, for the first time, in unstressed Si MOSFETs, where accumulation-mode, body-channel SOI MOSFETs are used [3-5]. It is revealed that worse μ_e in conventional inversion-mode Si MOSFETs is primarily due to larger D_{ac} at Si/SiO_2 interface [6] as well as the larger form factor induced by quantum confinement in 2D electron system.

2. Device structure

Fig. 1(a) shows the schematic of fabricated accumulation-mode, body-channel SOI MOSFETs with the same doping type in channel as that in the source/drain. Since there is no junction, drain current flows through the entire region of SOI layer at voltages around and higher than V_{FB} (**Fig. 1(b)**). Phosphorus concentration in SOI layer is 5×10^{15} cm^{-3}, as is confirmed by SIMS measurement (**Fig. 2**). T_{SOI} is in the range from 13 to 151 nm.

3. Mobility in body-channel SOI MOSFETs

Fig. 3 shows μ_e of 151 nm-thick, body-channel SOI MOSFET as a function of surface carrier concentration (N_s). The maximum μ_e of 1119 $cm^2V^{-1}s^{-1}$ is clearly confirmed. This is the record-high μ_e in unstressed Si MOSFETs. **Fig. 4** shows bulk Si μ_e as a function of doping concentration [1, 7]. μ_e of body-channel SOI MOSFET measured in this work is also indicated. It is demonstrated that μ_e of thick body-channel SOI MOSFETs is the same as bulk one.

4. Physical Mechanism of Higher Mobility

A. SOI thicknesses dependence

Fig. 5 shows the μ_e of body-channel SOI MOSFETs for various T_{SOI}. μ_e degrades gradually as T_{SOI} decreases from 71 nm. In **Fig. 6**, μ_e of body-channel SOI MOSFETs is compared with that of inversion-channel SOI MOSFETs for T_{SOI}'s of 13 nm and 71 nm. It should be noted that when T_{SOI} is approximately 15 nm, μ_e of body-channel MOSFETs is the same as that of inversion-channel MOSFETs. However, when T_{SOI} is approximately 70 nm, μ_e of inversion-channel MOSFETs is lower than that of body-channel MOSFETs. These results are explained by the difference in carrier distribution within the channel (**Fig. 7**). In the 15 nm T_{SOI} case, T_{SOI} is so thin that electron distributions are the same for both the body- and inversion-channel SOI MOSFETs. On the other hand, in the 71 nm T_{SOI} case, electrons populate more closely to the front MOS interface in the inversion-channel SOI MOSFETs; whereas electrons distribute more uniformly within the SOI layers in the body-channel SOI MOSFETs. These calculation results indicate that higher μ_e in thick body-channel SOI is due to the uniform carrier distribution in the thick body. The uniform carrier distribution may 1) decrease the form factor (a decrease in form factor increases μ_e), 2) decrease the impact of increased D_{ac} at MOS interface [6], and 3) decrease the effect of Coulomb scattering due to interface states. All these effects contribute to enhance μ_e.

B. Deformation Potential (D_{ac}) Contribution in High μ_e

In our previous work [6], we proposed the new D_{ac} model where D_{ac} increases sharply toward the Si/SiO_2 interface (**Fig. 8**). Therefore, average D_{ac} in body-channel SOI MOSFETs was considered to be lower than that in the inversion-channel SOI MOSFETs.

In order to confirm a decrease in average D_{ac} of body-channel MOSFETs, we investigated the strain effects on μ_e for both MOSFETs, since μ_e enhancement ratio ($\Delta\mu_e/\mu_e$) is proportional to D_{ac}. We applied uniaxial <110> tensile stress parallel to the channel and the μ_e enhancement ratio ($\Delta\mu_e/\mu_e$) was compared (**Fig. 9**). It is shown that the $\Delta\mu_e/\mu_e$ is smaller in body-channel SOI MOSFETs, indicating that D_{ac} in body-channel SOI MOSFETs is smaller than that in inversion-channel SOI MOSFETs. **Fig. 10** shows the $\Delta\mu_e/\mu_e$ for various substrate biases (V_b) in body-channel SOI MOSFETs. It is shown that $\Delta\mu_e/\mu_e$ is increased as the magnitude of negative V_b increases. This is because the depletion layer induced by V_b reduces the channel thickness, leading to an increase in average D_{ac}.

Finally, the effects of position dependent D_{ac} and wider wavefunction are more quantitatively studied by self-consistent calculations. The position dependent D_{ac} (**Fig. 11**), which is slightly modified from our previous report [6], is used to calculate μ_e of body-channel SOI MOSFETs (**Fig. 12**). It is shown that μ_e of body-channel SOI MOSFET is well reproduced by the model. By using the same D_{ac} model, we also reproduce the μ_e of inversion-channel SOI MOSFETs (**Fig. 13**). **Fig. 14** illustrates experimental and theoretical μ_e as a function of T_{SOI} in inversion-channel SOI MOSFETs [8], showing a good agreement. These results indicate the validity of our D_{ac} model. In other words, the observed record-high μ_e is due to a smaller average D_{ac} and smaller form factor in body-channel SOI MOSFETs.

5. Conclusions

We fabricated the body-channel SOI MOSFETs and observed the record-high μ_e of 1119 $cm^2V^{-1}s^{-1}$ in 151-nm-thick devices. This is due to a unique electron distribution in the body-channel SOI MOSFETs; electron distribute within the entire SOI layer, which leads to a smaller form factor, a smaller average deformation potential (D_{ac}), and less mobility degradation due to Coulomb scattering by N_{it}. From the stress effect on μ_e and the theoretical calculation of μ_e, the above model is confirmed (**Fig. 15**).

Acknowledgements
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References

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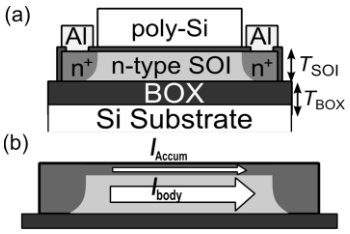

Fig. 1: (a) Schematic of accumulation-mode, body-channel SOI MOSFETs. The channel doping type is the same as the source/drain ones. (b) Current components in the device. At a voltage higher than V_{FB}, current flows in both the accumulation layer and body channel.

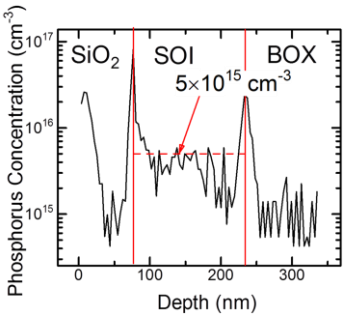

Fig. 2: Phosphorus SIMS profile in a 150 nm-thick body channel SOI MOSFET. Phosphorus concentration in SOI layer is determined to be 5×10^{15} cm^{-3}.

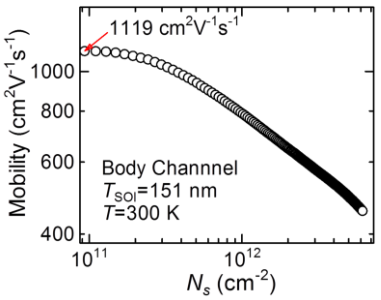

Fig. 3: Electron mobility (μ_e) of 151-nm-thick accumulation-mode, body-channel SOI MOSFETs. The observed μ_e of 1119 cm^{2}V^{-1}s^{-1} is the highest value among the values reported in unstressed Si MOSFETs.

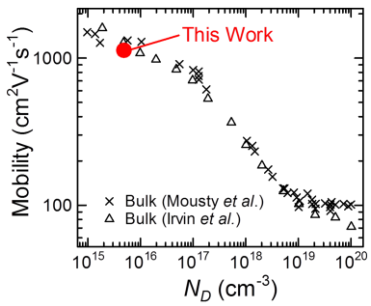

Fig. 4: Electron mobility (μ_e) as a function of donor concentration (N_D) in bulk Si. It is firstly demonstrated that μ_e of thick body-channel SOI MOSFET is the same as that of bulk Si.

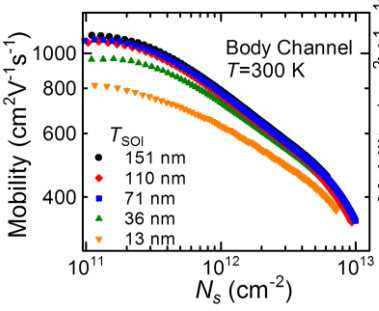

Fig. 5: Electron mobility (μ_e) as a function of surface carrier concentration (N_s) for various SOI thicknesses (T_{SOI}). It is confirmed that μ_e degrades when SOI thickness, T_{SOI}, is less than 71 nm.

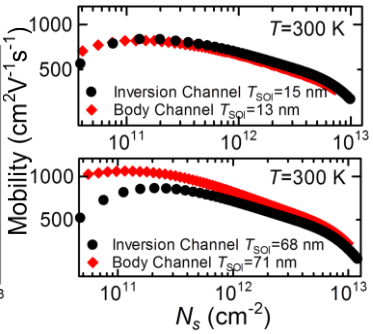

Fig. 6: Electron mobility (μ_e) for body-channel SOI MOSFETs in comparison with conventional inversion-channel SOI MOSFETs. The difference between two cases is obvious in thicker 70 nm-thick SOI MOSFETs.

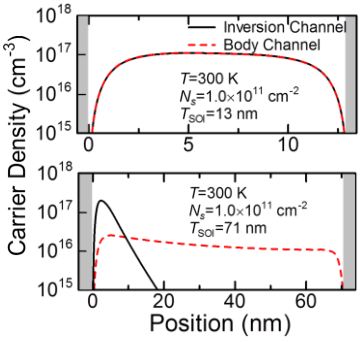

Fig. 7: Calculated carrier density for the body-channel and inversion-channel SOI MOSFETs. The carriers distribute in the entire SOI layer in 71 nm body-channel SOI MOSFETs, whereas the most carriers are located at the interface in inversion-channel MOSFETs.

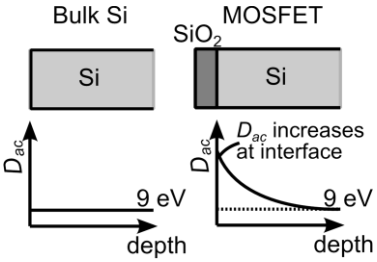

Fig. 8: Position-dependent deformation potential (D_{ac}) model proposed in Ref. 6. In bulk Si, D_{ac} takes the position-independent value of 9 eV. On the other hand, in MOS structures, D_{ac} increases sharply at Si/SiO_2 interface. In MOSFETs, electrons are concentrated more at the MOS interface, which leads to an increase in the average D_{ac} for electrons in MOSFETs.

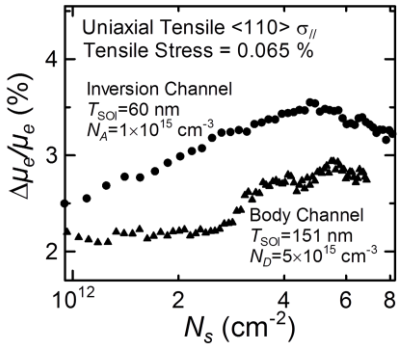

Fig. 9: Mobility enhancement ratio ($\Delta\mu_e/\mu_e$) induced by uniaxial tensile stress for body- and inversion-channel SOI MOSFETs. The smaller $\Delta\mu_e/\mu_e$ in body-channel SOI MOSFETs suggests that D_{ac} in body-channel SOI MOSFETs is smaller than that in inversion-channel SOI MOSFETs.

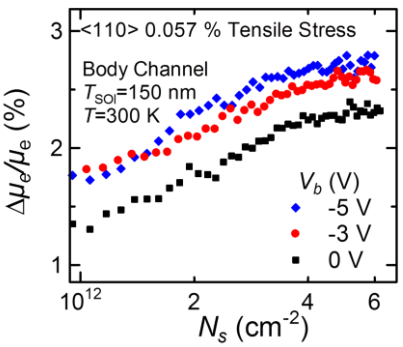

Fig. 10: Mobility enhancement ratio ($\Delta\mu_e/\mu_e$) induced by uniaxial tensile stress in body-channel SOI MOSFETs for various substrate biases (V_b). It is shown that $\Delta\mu_e/\mu_e$ increases as the magnitude of negative V_b increases.

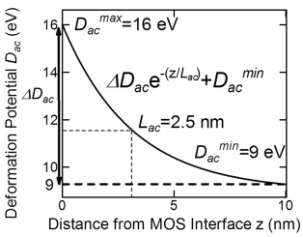

Fig. 11: D_{ac} at MOS interface. This position dependent D_{ac} is used to calculate μ_e shown in Fig.12-14.

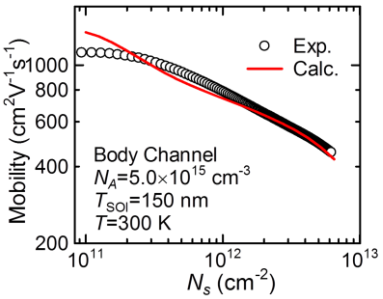

Fig. 12: Mobility (μ_e) versus surface carrier concentration (N_s) characteristics in body-channel SOI MOSFET. By using our position-dependent D_{ac} model, calculated μ_e agrees well with experimental data.

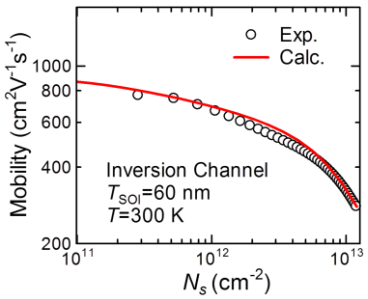

Fig. 13: Mobility (μ_e) versus surface carrier concentration (N_s) characteristics in inversion-channel SOI MOSFET. The good agreement between calculation and experiment is also confirmed in conventional, inversion-channel SOI MOSFETs.

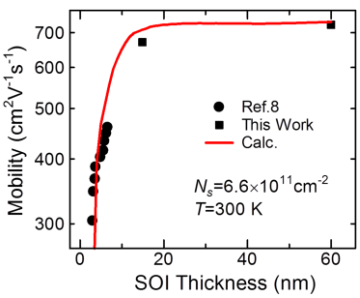

Fig. 14: Mobility (μ_e) versus SOI thickness (T_{SOI}) relationship in inversion-channel SOI MOSFETs at N_s of 6.6×10^{11} cm^{-2}. By using our position-dependent D_{ac} model, calculated μ_e agrees very well with experimental data over a wide range of T_{SOI}.

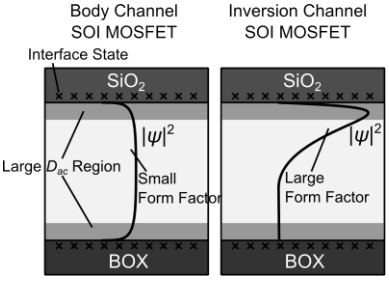

Fig. 15: The origin of mobility difference. In body-channel SOI MOSFETs, higher mobility is observed because of 1) smaller electron density in larger deformation potential region, 2) smaller form factor, and 3) less influence of interface states.