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On the understanding of mobility degradation mechanisms in advanced CMOS devices: FDSOI versus bulk technology

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Abstract

We investigate, in this paper, the mobility degradation mechanisms in advanced CMOS technologies. We highlight the impact of phonon, Coulomb and neutral defects scattering [1] on carrier's mobility degradation. This study was performed on N & PMOS Ultra Thin Buried Oxide Fully Depleted SOI (UTBOX FD-SOI) devices with two orientations, and on conventional Silicon bulk NMOS and SiGe bulk PMOS. UTBOX FD-SOI mobility was found to be higher in both N & PMOS compared to bulk technology for all the gate lengths and temperatures. The origin of this major improvement in SOI devices is clearly explained by the difference in phonon scattering at 300K (N and PMOS), Coulomb (NMOS and PMOS) and neutral defect (PMOS) scatterings at low temperature.

Device fabrication

The FDSOI devices were processed on 300mm not rotated and 45° rotated [2] UNIBOND^{TM} SOI wafers with a buried oxide thickness of 25nm. The final silicon film thickness under the gate is 8nm and the CET is around 17Å for PMOS and 16Å for NMOS for each substrate variant. The high-k is an HfSiON of 1.9nm combined with a 6.5nm thick PVD TiN. After the realization of an offset spacer of 8nm, a selective epitaxy of 16nm is performed in extension regions in order to reduce access resistance. Raised extensions are implanted. To finish a Dshape spacer, S/D implantation (activated by a 1080°C RTP spikes anneal) and silicidation (NiPtSi) are realized. Tensile Nitride layer has been added as contact etch stop layer. In addition, the use of UTBOX substrate combined with the Ground Plane leads to further SCE improvement [3] and additional V_T modulation [4].

Bulk studied devices were processed on 300mm (100) wafers, they have similar gate stack, Tinv=1.4nm for NMOS and Tinv=1.7nm for PMOS [5], with high-K dielectric on top of a SiON interfacial layer, and metal gate. PMOS transistors also have a SiGe channel.

Results and discussions

We first focused on <110> channel orientation SOI devices. The effective mobility μ_{eff} versus inversion charge (Figs. 1&2) extracted by the "split CV technique" reveals higher mobility in FDSOI devices compared to Bulk.

Id-Vg measurements were also performed in order to extract low-field mobility μ_0 for different gate length,

$$\mu_0 = \frac{L_{eff}\beta}{W_{eff}C_{ox}} \qquad (1)$$

Y function was used to extract the gain factor β [6] allowing the suppression of the contact resistance influence in individual transistors. The interest to focus on μ_0 remains in the fact that this parameter does not take into account the surface roughness effects on the mobility degradation.

Figures 3&4 show the low-field mobility versus effective gate length. As expected, FD SOI devices show an improvement of the μ_0 mobility up to 20% and 27% for N & PMOS respectively. This increase is attributed to the decrease of the effective filed in FD SOI devices compared to Bulk and to the doping absence.

For better understanding the difference in mobility between FDSOI and bulk, low temperature measurements were performed. An empirical model is used (2) to extract the different contributions of the low-filed mobility [7]. We tried to get closer to the experimental values as shown in Fig. 5.

$$\frac{1}{\mu_0}(T) = \frac{T}{300\mu_{ph}} + \frac{300}{T\mu_{cs}} + \frac{1}{\mu_N} \qquad (2)$$

in which μ_{ph}, μ_{cs}, μ_N correspond to the mobility due to phonon, Coulomb and neutral defect scattering, respectively. This equation takes into account the temperature dependence of μ_{ph}, μ_{cs} and its independence for μ_N as,

$$\mu_{0ph}(T) = \frac{300\mu_{ph}}{T} \qquad (3)$$

$$\mu_{0cs}(T) = \frac{T\mu_{cs}}{300} \qquad (4)$$

$$\mu_{0N} = \mu_N \qquad (5)$$

Figures 6&7 show the evolution of μ_{0ph}, μ_{0cs} and μ_{0N} with temperature in FDSOI and Bulk, N&PMOS. The main observation that we can notice, is that the phonon scattering seems to be the major mobility limitation factor in the two types of devices, and for instance, the impact of phonon is 99.5% larger than that of Coulomb scattering for FDSOI N and PMOS at 300K, and 92~96% larger in bulk N and P devices. On the other hand, the Coulomb scattering is increased in bulk MOSFETs by 95% in NMOS and 62% in PMOS, and the phonon scattering is enhanced by 25% in NMOS and 50% in PMOS compared to SOI technology.

These data highlight also the efficiency of SOI devices in term of Coulomb scattering reduction, which is indeed related to channel doping reduction in FDSOI. We also observe, that the neutral defect and phonon mobility seem to have more effects in bulk SiGe PMOS, leading to a reduction of 72% for μ_N and 50% for μ_{ph} compared with SOI devices (Fig. 7).

At low temperature, because phonons scattering is reduced, the neutral and Coulomb scatterings become the main mobility limitation for bulk and SOI MOSFETs (Figs. 6,7).

One can also notice the hole mobility increase due to channel direction <100> as shown in Fig. 8 for PMOS FDSOI [2]. However, at very low temperature this tendency is reversed because of the Coulomb scattering mechanism, which becomes more important for <100> orientation, with a reduction of μ_{cs} by 75 % compared with <110> orientation (Fig. 9). This phenomenon is induced by the channel scaling down (35 nm) and Source/Drain implant.

Conclusions

We compared, for the first time, the low-field mobility in Bulk silicon NMOS, SiGe PMOS and FDSOI N & PMOS devices with different orientations. Low temperature measurements were performed to understand the main scattering mechanisms that govern carrier's mobility. The origin of the major mobility improvement in SOI devices is clearly explained by the difference in phonon scattering at 300K with the decreasing of the effective field (N and PMOS). And at low temperature, the decreases of the Coulomb scattering (NMOS & PMOS) by the doping absence and finally, neutral defect (PMOS) scatterings.

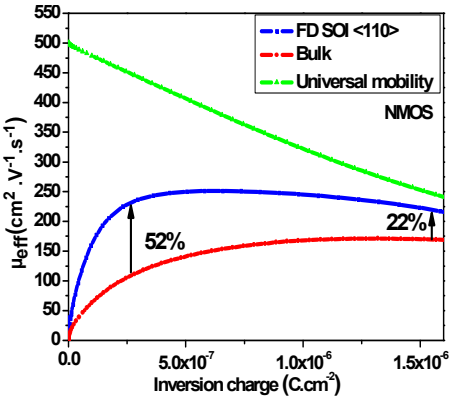

Figure 1 :Effective mobility vs inversion charge for NMOS WxL=10µmx10µm

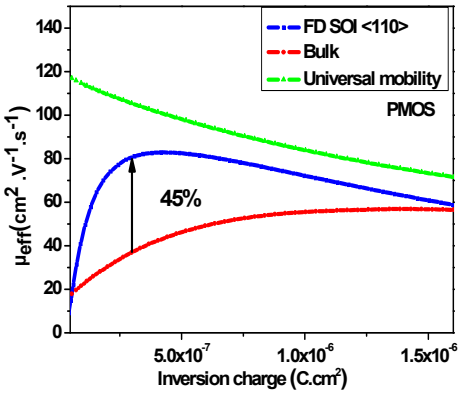

Figure 2 :Effective mobility vs inversion charge for PMOS WxL=10µmx10µm

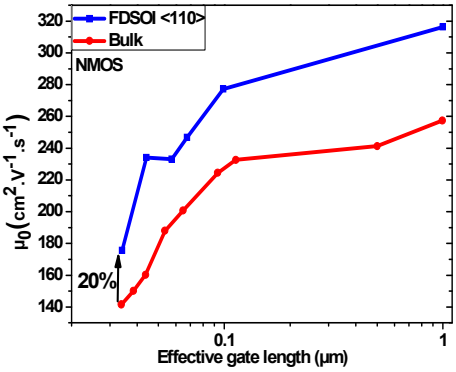

Figure 3: Low-field mobility vs effective gate length for NMOS FD SOI & Bulk devices

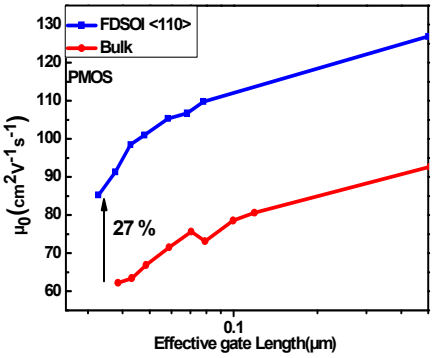

Figure 4: Low-field mobility vs effective gate length for PMOS FD SOI and SiGe Bulk devices

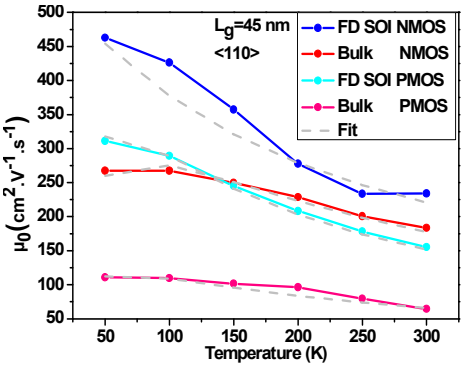

Figure 5: Low-field mobility vs temperature for N&PMOS

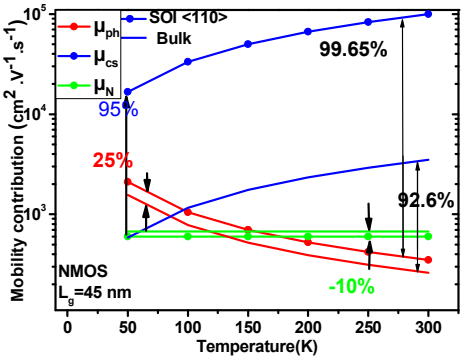

Figure 6: Mobility contribution vs temperature for NMOS Lg=45 nm

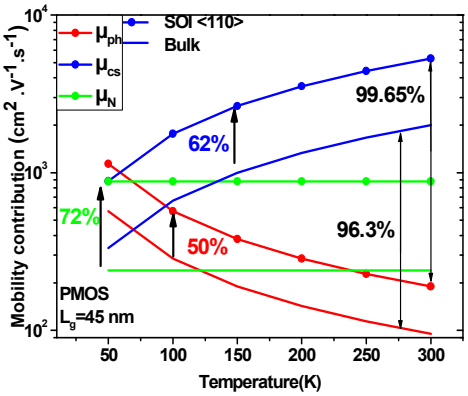

Figure 7: Mobility contribution vs temperature for PMOS Lg=45 nm .

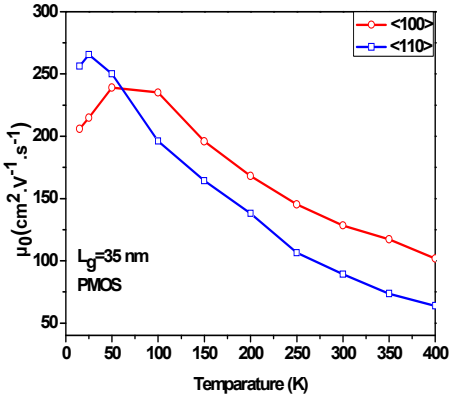

Figure 8: Low-field mobility vs T(K) for PMOS FD SOI for (100) and (110) wafer orientation

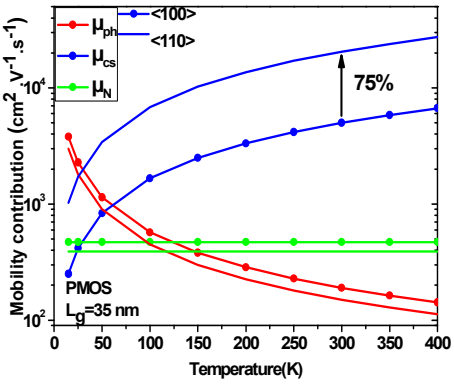

Figure 9: Mobility contribution vs T(K) for 35 nm PMOS FD SOI for (100) and (110) wafer orientation

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