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$Si_{1-y}Ge_y$ or $Ge_{1-z}Sn_z$ Source/Drain Stressors on Strained $Si_{1-x}Ge_x$-Channel PFETS: A TCAD Study

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1. Introduction

$Si_{1-x}Ge_x$-channel pFETs can be used to further enhance performance of CMOS technology. Properties of this technology are: improved scalability and mobility [1, 2], further performance enhancement for narrow-width pFETs due to uniaxial channel stress [3], compatibility with other stressors like $Si_{1-y}Ge_y$ source/drains [4] and superior negative-bias temperature instability [5].

The combination of a strained channel and a source-drain stressor leads to a different optimization than for silicon-channels: whereas for Si-channels the recess depth of the S/D module needs to be maximized for the highest stress, for SiGe-channels, less recess may lead to higher final channel stress, especially for short channels [2, 6]. The goal of this abstract is to give a more complete analysis of how the combination of the channel- and source/drain-stressor module can be optimised in gate-first and gate-last technologies.

Stress simulations are performed either in Taurus-Process [7] or Sentaurus-Process [8]. Positive stress values indicate tensile stress, negative stresses are compressive. As this work focuses on the stress from the buffer and source/drain stressors, all other layers are deposited without intrinsic stress.

2. $Si_{0.45}Ge_{0.55}$-channel PFETs on a silicon substrate with $Si_{0.75}Ge_{0.25}$ source/drains: effect of recess depth

This section studies the effect of source/drain recess depth on channel stress. A typical cross-section with all relevant dimensions is shown in Figure 1. $Si_{0.45}Ge_{0.55}$-channels are deposited, strained w.r.t. the underlying silicon substrate. The main parameters that are varied are the gate length and the source/drain recess depth: the latter is varied between 0 nm (no recess) and 60 nm. An important intermediate case for the recess depth is 5 nm: in this case only the Si-cap and $Si_{0.45}Ge_{0.55}$-channel are etched out, but no material of the Si substrate underneath. In all cases the source/drain overgrowth is kept constant at 30 nm above the original silicon level.

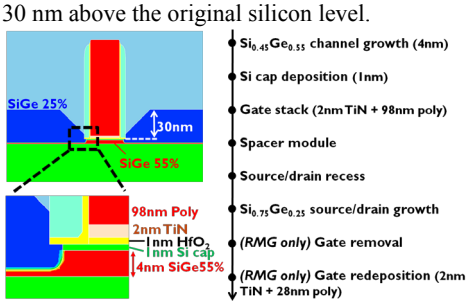

Figure 1. Cross-section after the gate-first module of $Si_{0.45}Ge_{0.55}$-channel FETs with a $Si_{0.75}Ge_{0.25}$ source/drain. All simulations use a gate pitch of 1 micron.

Figure 2 (top-left) shows the longitudinal stress in the $Si_{0.45}Ge_{0.55}$ channel after the recess etch of the source/drain module. The spacer width is kept constant at 6 nm. Recess leads to elastic relaxation of the stress, an effect that becomes more significant for shorter channels and deeper etch. However, once the recess is deeper than the $Si_{0.45}Ge_{0.55}$ channel (> 5 nm recess depth in Figure 2, top-left) the further effect on stress relaxation is limited.

The channel stress after source/drain epitaxial growth is shown in Figure 2 (top-right), indicating that for a gate-first process, a deeper recess leads to the highest stress for longer channels (gate length > 20 nm), while for short-channel pFETs a raised source/drain (recess 0 nm) is more beneficial. The lowest efficiency for the source/drain module is obtained for 5 nm recess, i.e. the case where only the channel and Si-cap are removed.

Figure 2 (bottom-left) shows that gate removal leads to strong further enhancement of the channel stress w.r.t. gate-first. Moreover, also in the gate-last case it is less beneficial to use a very deep source/drain recess at gate lengths below 30 nm. Plotting the stress versus recess depth (Figure 2, bottom-right) confirms this: for short channels, similar channel stress can be obtained either by a very deep recess, or by omitting the S/D etch altogether.

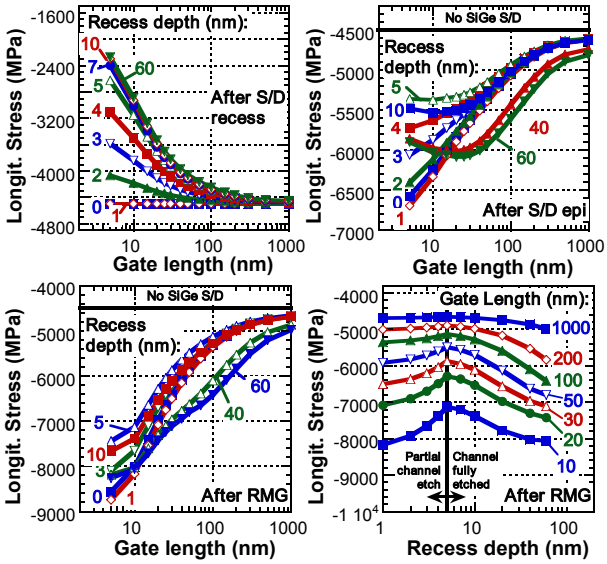

Figure 2. Longitudinal stress in the center of the channel for $Si_{0.45}Ge_{0.55}$-channel FETs with a $Si_{0.75}Ge_{0.25}Ge$ source/drain. (Top-left) After source/drain recess. (Top-right) After source/drain epitaxial growth. (Bottom-left) After gate-last module. (Bottom-right) Versus recess depth, after gate-last module. Spacer width is kept constant at 6 nm.

If the source/drain stressor is highly doped, having a spacer width of 6 nm might lead to loss of short-channel control for deeply recessed source/drain stressors. As a consequence there is a trade-off between spacer width and recess depth. Figure 3 shows an example where the spacer width needs to be linearly scaled with recess depth. As a deeper recess is now further away from the channel, it leads to less stress relaxation after recess (Figure 3, top-left), but also to less additional stress coming from the source/drain epi, resulting in a similar stress after epigrowth than for the constant-spacer case (Figure 3, top-right). For gate-last transistors, a deep recess is again found to be preferred for long channels (Figure 3, bottom-left). Zero

recess provides a valid alternative for short-channels (Figure 3, bottom-right), and might be the preferred choice in terms of layer stability. Overall channel stresses in the order of several gigapascals are found, values that can only be achieved if the channel is sufficiently thin and of excellent epitaxial quality.

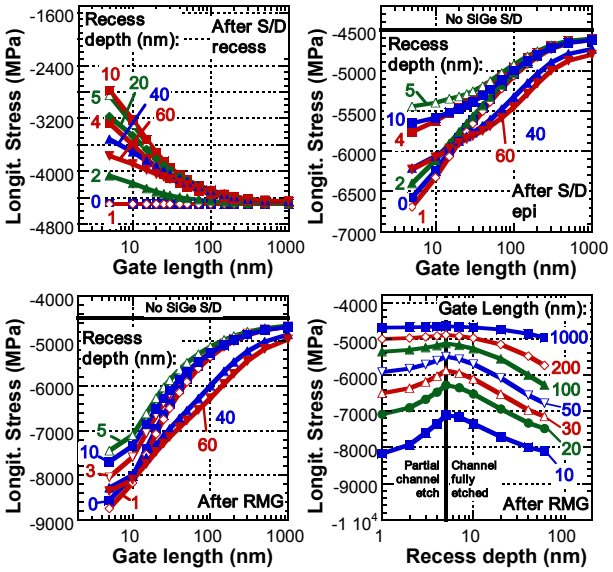

Figure 3. Longitudinal stress in the center of the channel for $Si_{0.45}Ge_{0.55}$-channel FETs with a $Si_{0.75}Ge_{0.25}Ge$ source/drain. (Top-left) After source/drain recess. (Top-right) After source/drain epitaxial growth. (Bottom-left) After gate-last module. (Bottom-right) Versus recess depth, after gate-last module. Spacer width is scaled linearly with recess depth: between 6 nm spacer width for 0 nm recess and 20 nm width for 60 nm recess.

3. Ge-channel PFETs on $Si_{1-x}Ge_x$ Strain-Relaxed Buffers (SRBs) with $Si_{1-y}Ge_y$ or $Ge_{1-z}Sn_z$ source/drains

This section looks at the effect of the stressor concentration (Ge % in the SRBs and Ge or tin % in the source/drain region) for germanium-channel pFETs. Short-channel transistors with gate lengths of 20 nm and 6 nm-wide spacers are simulated. The source/drain module has no recess and an overgrowth of 30 nm. $Ge_{1-z}Sn_z$ is modeled as a material that provides 1.7 % mismatch w.r.t. Ge for each 10 % of tin, based on [9]. Figure 4 shows an overview of the simulation setup.

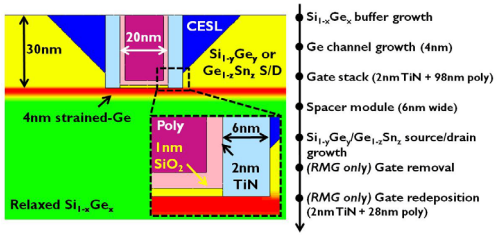

Figure 4. Cross-section after the gate-last module of strained-Ge channel FETs on a relaxed $Si_{1-x}Ge_x$-virtual buffer with a $Si_{1-y}Ge_y$ or $Ge_{1-z}Sn_z$ source/drain. All simulations use a gate pitch of 1 micron.

Figure 5 shows the stress in the channel center when two stressors are combined, an SRB and a source/drain module. For pFETs, a compressive/negative longitudinal stress is preferred for mobility enhancement. Higher compressive channel stress can be obtained by decreasing the germanium concentration in the SRB and increasing the germanium/tin concentration in the source/drain. The dashed black line connects points that show the effect of the SRB only (i.e. equal Ge % for the SRB and S/D modules, leading to no additional stress from the S/D). The SRB-only channel stress is found to be very large and independent of whether a gate-first or -last scheme is used (black line, Figure 5, top versus bottom). For a $Si_{0.25}Ge_{0.75}$ or $Si_{0.5}Ge_{0.5}$ SRB, a germanium source/drain already leads to significant additional stress. Adding tin in the source/drain regions can be used for further mobility enhancement. This is especially interesting for gate-last technologies, as in this case source/drain stressors are more effective (slope of the curves in Figure 5, top versus bottom).

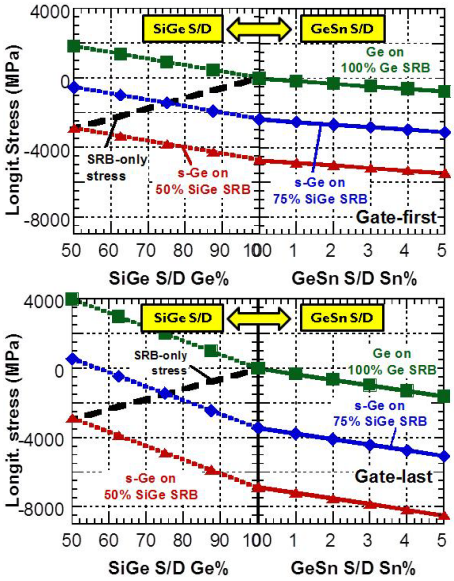

Figure 5. Longitudinal channel stress versus Ge or Sn % in the source/drain module for Ge-channel FETs. (Top) Gate-first FETs. (Bottom) Gate-last FETs.

4. Conclusions

This abstract studies the effect of a source/drain stressor and a strain-relaxed buffer on strained $Si_{1-x}Ge_x$-channel pFETs for gate-first and gate-last technologies. While for long channels, deeper recess leads to higher stress, for short-channel FETs leaving the $Si_{1-x}Ge_x$ untouched and opting for a raised S/D approach leads to similar or higher channel stress and may be the preferred option from layer-stability point of view.

The combination of $Si_{1-x}Ge_x$ SRBs and tin-doped germanium source/drains is found to be efficient to further boost mobility of germanium-channel pFETs, especially in combination with gate-last technologies.

Acknowledgements

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References

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