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Design-friendly scalability of cost-effective 28LP technology platform featuring 2nd generation gate-first HK/MG transistors without *e*SiGe

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1. Introduction

A manufacturable LP technology platform has been scaled down to the 32/28nm node [1]. It has been attempted to maintain the device performance even with a short gate-to-gate pitch (C_{pp}) by various method, *e.g.*, a HK/MG stack [2-5], embedded SiGe source/drain (*e*SiGe) [6-8] and their combination [9]. However, such boosting processes often require the restriction rule of circuit design like a uni-directional layout of the gate electrode. Moreover, the circuit designers might again suffer from the major change of their designs due to emergence of the FinFET beyond 14nm node. As a result, it is a reasonable scenario for saving the design cost to extend the conventional circuit design as much as possible until the technology jump to the FinFET. From this viewpoint, the gate-first HK/MG technology without the *e*SiGe is a good candidate because of its design flexibility related with a simple fabrication procedure. In contrast, such simple device architecture had limited its performance, in particular, for the PFET. In this study, we have improved 28nm LP device performance by simple and scalable methods and have comprehensively investigated the scalability of cost-effective 28nm LP technology to continuously provide the design-friendly environment.

2. Results and discussion

Gate pitch scalability

Since the narrower C_{pp} decreases the junction leakage current whereas the CESL-induced stress becomes the weaker, it is possible to suppress the NFET performance degradation induced by scaling the C_{pp}. By optimizing both the junction profile and stress transfer efficiency, the CESL with a higher tensile stress became effective to improve the NFET performance even for the narrow C_{pp}. In contrast, the narrower C_{pp} simply enhances the PFET performance by relaxing the CESL stress. Moreover, the PFET performance was improved by the gate stack engineering, which is independent of the gate pitch. Consequently, it is considered that the gate pitch scaling with maintaining the performance would be possible for the gate-first HK/MG device if the lithography technique would be prepared.

2nd generation gate-first HK/MG device

We have achieved the N-/PFET I_{dsat} of 1.32/0.67 and 0.91/0.47 mA/μm with the I_{off} of 100 and 1 nA/μm for the V_{dd} of 1V, respectively (Fig. 1). The high tensile CESL and new HK/MG stack dominantly improved the device performance by 10% for N- and PFETs, respectively. The HK/MG stack was simply modified to control the trap states and reduce the IL bottom roughness. The new HK/MG stack enhanced both the drive (6%) and linear currents (8%) with less shift in the threshold voltage (V_t) for all the transistors with various gate size. What is interesting is that this improvement is not caused by mobility enhancement but by increase of the carrier concentration in the overlapped extension region because the trap state density near the extension region was reduced. Moreover, the flatter IL bottom improved the PFET performance by 4%. Since such gate stack engineering did not affect the NFET performance, we simply achieved the improvement of 10% in PFET performance at the C_{pp} of 114nm.

Scalability of the gate length and width

Although it had already been reported that the gate-first HK/MG device had a good intrinsic local variability [2], the advanced HK/MG stack enables such local variability to be additionally reduced. Figure 2 shows the local V_t fluctuations extracted by the neighboring pair transistors. The advanced HK/MG stack decreased the A_{Vt} by 6 and 8% for N- and P-FETs, respectively. The extracted amounts of the A_{Vt} were 1.45 for the NFET and 1.55 for the PFET. On the basis of the scaling trend of the SRAM cell size against the A_{Vt}, we could expect to additionally shrink the SRAM cell size by 6% without degradation in static noise margin. As a result, since the local V_t fluctuation is sufficiently good for the 2nd generation HK/MG devices, the concern by scaling the gate size might be the performance degradation. Then, we investigated dependence of the N- and PFET performance on the gate width (W_g) with the C_{pp} of 114nm. It was found for both N- and P-FET that the on-current (I_{on}), which is defined as the I_{dsat} with the I_{off} of 1nA/μm at the V_{dd} of 1V, monotonously increased when the W_g was decreased to 70 nm without an increase of the minimum gate length with the I_{off} of 1nA/μm (L_{min}). As a result, it is considered that our 28nm LP technology has a good capability for scaling the gate area size with less degradation in the device performance.

Scalability of the active area size and its pitch

In order to shrink the size of the active region, it is also important to decrease the lateral length of the active region (LOD) in addition to the width corresponding to the W_g. It has already been reported that the LOD scaling without dummy gates results in the serious degradation in the PFET with the *e*SiGe due to the reduction in its volume [10]. In contrast, our gate-first HK/MG device is almost the free

from this issue because there is no *e*SiGe. It was found that the I_{on}-I_{off} characteristic was almost the same between the LODs of 3000nm and 167 nm, which makes the neighboring gate completely locate on the shallow trench isolation beyond the edge of the active region at the C_{pp} of 114nm. This result suggests us that the LOD is scalable for the PFET without undesirable dummy gates at the edge of the active region. The reduction in the pitch of the active region is also important to increase the density of the transistor. We found that the simple spacer scaling enables the increase of 15% in the transistor density with the performance degradation of a few percent, which might be easily compensated. Consequently, it is considered that the active region and its pitch are also scalable into the limit of the lithography resolution for the gate-first HK/MG devices with maintaining the performance.

Flexibility of the gate layout

One of the most attractive points for the gate-first HK/MG technology must be the flexible layout of the gate electrodes without the uni-directional restriction. It is expected to be possible to maintain such flexibility even after shrinking the device size. For example, we evaluated the V_t shift as a function of the distance between the vertical gate and active edge in the finger transistor. We found that it is possible to reduce the systematic V_t shift by process optimization without changing a lithography mask for the gate patterning. Therefore, it is considered that various gate layout would be available with the tighter proximity from the gate to active region for the gate-first HK/MG device with the relatively simple fabrication procedure of the gate.

3. Conclusions

Scalability of the 28nm gate-first HK/MG LP devices with maintaining the performance and layout flexibility was comprehensively studied for the first time. We demonstrated the competitive performance by the 2nd generation gate-first HK/MG devices, which are designed to be suitable for simply scaling the circuit area. It was found that the size and pitch of gate electrodes are scalable from the viewpoints of the performance and variability. In addition, we found that both the size and pitch of active region are also scalable. Moreover, it is expected to keep the flexible gate layout without serious systematic Vt shift. Consequently, we consider that the 28nm LP technology platform featuring the gate-first HK/MG devices would be additionally scalable with keeping the device performance and design-friendly device layout rule to save the design cost by maintaining the legacy from the previous generations.

References

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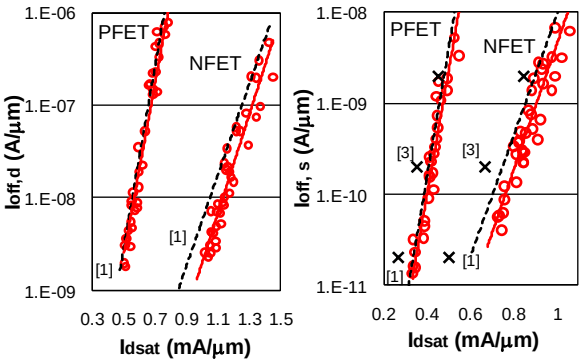

Fig. 1 Idsat-Ioff of HP and LOP transistors with 2nd generation gate-first HK/MG. Vdd=1.0V. Cpp=114nm.

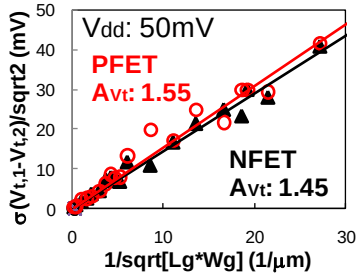

Fig. 2 Local fluctuation in threshold voltage among transistors with 2nd generation gate-first HK/MG. Vdd=0.05V. Cpp=114nm.

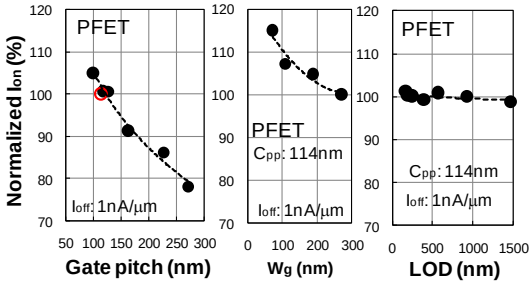

Fig. 3 Dependences of the on-current on key layout factors (Cpp, Wg and LOD) for PFETs with 2nd generation gate-first HK/MG. Vdd=1.0V.