Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials, Kyoto, 2012, pp819-820

Analysis of Read Margin Improvement for Low Voltage SRAM Composed of Nano-Scale MOSFETs with Ideal Subthreshold Factor and Small Variability

Chika Tanaka, Masumi Saitoh, Kensuke Ota and Toshinori Numata
Advanced LSI Technology Laboratory, Corporate R&D Center, Toshiba Corporation
8 Shinsugita-cho, Isogo-ku, Yokohama 235-8522, Japan
Phone: +81-45-776-5958 E-mail: chika.tanaka@toshiba.co.jp

1. Introduction

Si nanowire transistors (NW Tr.) are promising device structures for further scaling [1]. The ideal subthreshold characteristic of NW Tr. is a key to maintain high I_{on}/I_{off} ratio in low voltage operations of CMOS logic circuits [2]. NW Tr.-based SRAM cell is also applicable to the low power memory with the low supply voltage (V_{dd}). V_{dd} scaling of SRAM is limited by the threshold voltage variations. It has been demonstrated that DIBL should be suppressed to keep the mean static noise margin (μSNM) high even at low V_{dd} in bulk MOSFETs [3]. However, the performance of SRAM composed of MOSFETs with the ideal *S*-factor has not been fully examined yet. In this study, SPICE simulations for NW-Tr. SRAM are performed on the basis of the measurement data. The impact of *S*-factor on SRAM SNM and the minimum operating voltage (V_{ddmin}) is evaluated in NW Tr. as well as in quasi-planar bulk Tr. (Bulk+ Tr.).

2. Simulation methods

Device structures and characteristics

Fig. 1 shows the schematic device structure and the cross-sectional TEM image of NW Tr. Tri-gate NW Tr. with various channel length (L_g) and NW width (W_{NW}) were fabricated on 300mm SOI wafers. Poly-Si gate and SiO_2 gate stack and undoped nanowire channel were adopted in the fabrication. We have demonstrated that the systematic study of V_{th} and I_d variability of NW Tr. with various parameters in Pelgrom plot [4] and verified that the device mismatch coefficient (A_{vt}) of NW Tr. is lower than that of planar Tr. [5]. In order to evaluate the impact of subthreshold characteristics on SRAM performance, BSIM4 was used to follow the device characteristics with different *S*-factor. Fig. 2 (a) and (b) show the schematic device structure of bulk planar Tr. (Bulk Tr.) and Bulk+ Tr, respectively. Bulk+ Tr. exhibit steeper subthreshold slopes due to better gate-to-channel capacitive coupling [6]. I_{off} of all devices were set to be HP/LOP/LSTP conditions reported in ITRS 2011 [7].

SPICE parameter extraction for NW Tr.

UTMOST IV [8] was used to extract the SPICE model parameters of BSIM4 from the measurement data of NW Tr. Fig. 3 shows the typical results of the simulated I_d-V_g/I_d-V_d curves and the measurement results. Good fitting with maximum error < 3% was achieved for both *n*- and *p*-channel Tr. with sub-100nm gate length.

3. Impact of *S*-factor on SRAM SNM

Fig. 4 shows the schematic of SRAM cell circuit. SNM was defined as the side length of square of SRAM butterfly curve, plotting the voltage transfer characteristics of two inverters [9]. Fig. 5 shows SNM of NW Tr.-based SRAM with 20nm and 100nm-W_{NW} against I_{off}. V_{dd} was set to be 0.5V. *S*-factor of NW Tr. with 20nm-W_{NW} and 100nm-W_{NW} are 65 and 81mV/dec, respectively. It is found that SNM of W_{NW} of 20nm increases higher than that of wide W_{NW}. The ideal *S*-factor is a key factor for the high SNM with sufficient gate voltage at low V_{dd}.

Fig. 6 shows SNM of Bulk/Bulk+/NW-Tr.-based SRAM plotted as a function of V_{th} for pull-down (PD) transistor. When V_{th} increases, SNM also increases. However, SNM of Bulk+/NW Tr. are higher than that of Bulk Tr. at the same V_{th}. As shown in Fig.7 (a), steep subthreshold slope with high I_{on}/I_{off} ratio is required to reduce V_{dd}. When V_{dd} decreases, I_{on}/I_{off} ratio of NW Tr. is kept higher than that of Bulk Tr. because of the ideal subthreshold slope. As shown in Fig.7 (b), higher V_{th} for *n*MOSFET is beneficial to obtain high SNM and higher I_{on} is required to pull down the output voltage to low level. Fig. 8 shows the relationship between SNM and I_{on}/I_{off} ratio of PD transistors with the same V_{th}. SNM increases as I_{on}/I_{off} ratio increases. Therefore, I_{on} is the major factor in the improvement of SRAM cell stability. This result confirms that the ideal subthreshold slope, which realizes high I_{on}/I_{off} ratio, is a key for the enhancement of SNM with low V_{dd} SRAM operations.

4. Influence of V_{th} variability on SRAM performance

SRAM stability is seriously affected by the V_{th} variation ($\sigma\Delta V_{th}$) of transistors. Fig. 9 shows the maximum A_{vt} (A_{vt}^{max}) for V_{dd}=0.5V, which guarantees the read/write margin with 6σ yield requirement of SRAM cell. The typical values of A_{vt} for the different transistors are also plotted. Smaller A_{vt}^{max} of Bulk Tr. makes a read operation fail. Fig. 10 shows the relationship between V_{ddmin} and A_{vt}. Since the scaling limits of operation voltage are determined by the typical A_{vt}, V_{ddmin} of Bulk+ Tr. is 600mV smaller than that of Bulk Tr. due to the steep subthreshold slope with high I_{on}/I_{off} ratio. It is found that the reduction of V_{th} variation is required for more aggressive voltage scaling, meaning that NW Tr.-based SRAM has a promising performance from the points of not only steep *S* factor, but also the robustness for V_{th} variation.

5. Conclusions

The read stability for low voltage SRAM with different *S*-factor was investigated. The ideal subthreshold slope characteristic is a key to maintain I_{on}/I_{off} with respect to obtain the large μSNM in low V_{dd} as well as low I_{off}. These results suggest that NW Tr.-based SRAM cell is applicable to the low power memory even in low operating voltage.

Acknowledgements
This work was partly supported by NEDO's Development of Nanoelectronic Device Technology.

References

[1] M. Saitoh *et al*., VLSI Tech. Dig., p.169 (2010). [2] C. Tanaka *et al*., ESSDERC, p.159 (2011). [3] F. Tachibana *et al*., SSDM, p.192 (2004). [4] M. J. Pelgrom *et al*., IEEE JSSC, 24, p.1433 (1989). [5] M. Saitoh *et al*., VLSI Tech. Dig., p.132 (2011). [6] C. Shin *et al*., IEEE Tran. ED, 58, p.1846 (2011). [7] ITRS, http://www.itrs.net/. [8] Silvaco, http://www.silvaco.com/. [9] E. Seevinck *et al*., IEEE JSSC, 22, p.748 (1987). [10] T. Chiarella, *et al*., ESSDERC, p.85 (2009)

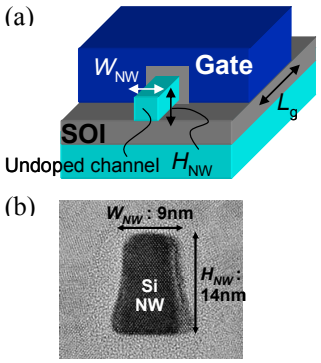
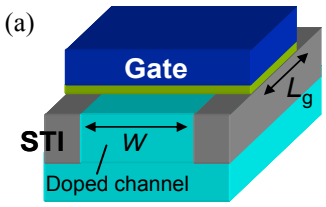


Fig.1 (a) The schematic device structure and (b) the cross-sectional TEM image of NW Tr.



S-factor (n/p)	W(nm)
86/83	200

S-factor (n/p)	W(nm)	H(nm)
67/67	50	20

Fig.2 The schematic device structure of (a) planar bulk Tr. (Bulk Tr.) and (b) quasi-planar bulk Tr. (Bulk+ Tr.)

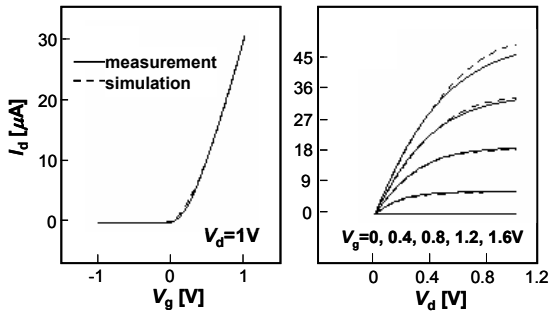


Fig. 3 The simulated versus measured I_d-V_g/I_d-V_d curves for n-type NW Tr. with W_{NW}=20nm, H_{NW}=20nm and L_g=80nm.

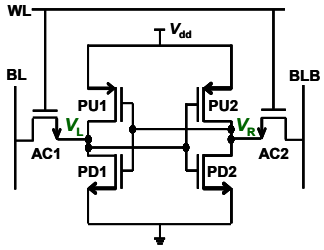


Fig.4 The schematic of 6T-SRAM cell circuit.

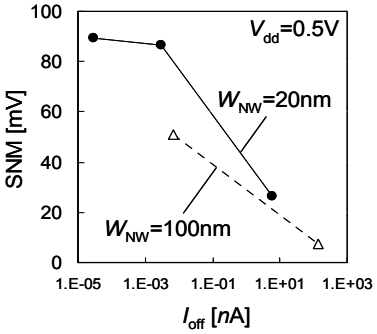


Fig.5 NW-Tr.-based SRAN SNM with 20nm- and 100nm-W_{NW} against I_{off}. H_{NW}=20nm and L_g=80nm.

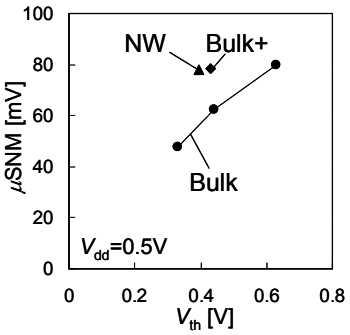


Fig. 6 SNM at V_{dd}=0.5V are plotted as a function of V_{th} of PD transistor. L_g of all devices are 50nm.

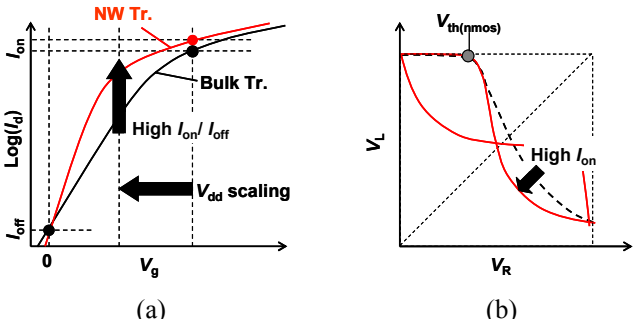


Fig. 7 (a) The switching characteristics of MOSFET and (b) voltage transfer curve of the internal inverters of SRAM.

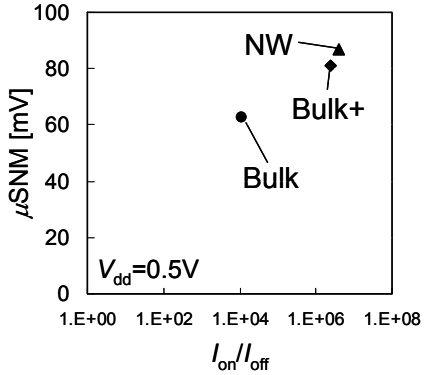


Fig. 8. μSNM at V_{dd}=0.5V are plotted as a function of I_{on}/I_{off} of PD transistor with the same V_{th}.

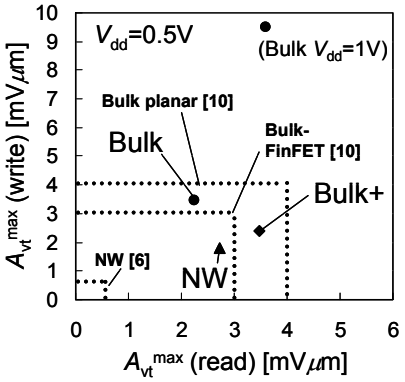


Fig. 9 Maximum A_{vt} for read/write operations at V_{dd}=0.5. Dotted lines indicate the typical A_{vt}.

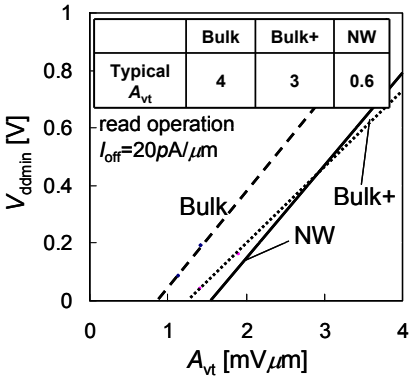


Fig. 10 Relation between V_{ddmin} and A_{vt} for read operation with low off current.