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A Comparative Study of Minimal Supply Voltage of 6T-SRAM at the 16nm node using MASTAR into a Conventional CAD Environment

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Introduction

In advanced CMOS technology, the choice of the device structure is driven by two key parameters: the logic performance (inverter delay) and the SRAM performance (SNM). In this paper we will focus only on variability robustness at the 16nm in SRAM cells. Bulk, FDSOI and SOI-FinFET structures (Fig. 1) will be compared using the MASTAR model [1] improved and implemented in VerilogA language to be able to use CAD tools, such as ELDO [2].

Model and methodology description

To provide a predictive and universal (i.e. valid for all structures) MOSFETs model, we use the VDT [3] to compute electrostatic parameters of each device structure [4, 5]. For the drain current, we use a drift-diffusion model, based on universal mobility law [6]. To ensure the continuity in all regions, mandatory for CAD tools, we use effective gate and drain voltages as in [7, 8]. Intrinsic charges expressions are obtained as in [8] and parasitic capacitances (extrinsic charges), are implemented using [9]. Then, to perform predictive circuit simulations with ELDO, such as SRAM, we implement it in VerilogA. To account for variability, we define process parameters local variation distribution, such as gate length, and run simulation with ELDO which generates pseudo random values of those parameters, following their distribution law.

Studied devices definition

First, we define a performance target common to each structure for the 16 nm node. We start from the performance demonstrated by typical 20nm node bulk devices [10] and consider that the performance should be 20% higher in I_{on} for same I_{off}. We choose to fix I_{off} at 5nA/µm, leading to a I_{on} specification at 1104 µA/µm for NMOS and 1032µA/µm for PMOS (Fig. 2). Then, for each structure, we set the Contacted Poly Pitch (CPP) at 64 nm (according to the Moore's law, CPP is divided by ~2 every two nodes and CPP=126nm for 32 nm node in [11]), the gate length of logic device (L) to 20nm and the power supply V_{dd} at 0.8V (i.e. 100mV reduction from 0.9V for the 20nm node [10]). Then, we used the "good technology rules" described in [4] to set the channel thickness in FDSOI and FinFET cases. Finally, for FinFET devices, we used the ratio h_{si}/t_{si}=2.5 from [12]. Dimensions and static performances of each device are summarized in Table 1. In order to reach the performance targets defined above while using the proper device geometry, we adjusted the strain behaviour and the series resistance for all the architectures. It is worth noticing that Bulk device cannot achieve the desired level of specification at the targeted leakage, which has to be relaxed by a factor of 20x.

Layout definition

By extrapolating the industry trend of SRAM bit-cell area from the last years (65nm-28nm), we found that at 16nm node the bit-cell area should be around 0.04~0.045µm². SRAM transistors layout, i.e. width and gate length of each transistor (Fig.3) are then defined by targeting at the same time a final area within this limit, but also a Static Noise Margin (SNM, defined on Fig 4) around 185 mV at the nominal V_{dd} (0.8V). This value is typical of what could be expected from a proper trade-off between read and write ability of the SRAM [13]. The bit-cell area can be expressed as $L_{cell}xH_{cell}$, with:

$$L_{cell} = 2(W_{PD} + W_{PU} + L_c + \frac{A2A}{2} + W_{ext} + \frac{PS}{2} + NP) \quad (1)$$

$$H_{cell} = 2(L_{PD} + \frac{L_c}{2} + C2G) \quad (2)$$

With L_c, A2A, W_{ext}, PS, C2G, and NP the distance defined on Fig.3. To estimate those dimensions, we extrapolate the simple expressions of [9] to SRAM cell and summarize them in Table 2. For planar structures (i.e. Bulk and FDSOI) each dimension is freely adjustable. But for FinFET we have to face the issue due to discrete width. In our case, as h_{si}=25nm, the device width increases by step of 60nm ($2h_{si}+t_{si}$) for each additional fin. Because of our SNM target (185mV@Vdd=0.8V), we have to use a layout with only one fin for each device, and so, the same device width. Consequently, the adjustment of the SNM has been carried out only with gate length variation. Layout, area and SNM obtained are summarized in Table 3 and the SNM(V_{dd}) curve is presented on Fig. 6.

Variability sources definition

To benchmark the robustness to variability of each device structure, we include local variations of gate length (L), device width (W), film thickness (t_{si}), gate workfunction (φ_m) and channel doping (N_{ch}). We consider that these variations are Gaussian and we summarized the standard deviation of each parameter, estimated in accordance with literature [14-16] in Table 4. Note that for etched-based process we considered the CD variation to be : $3\sigma_{CD}=12\%_{CD}$ We ran ELDO simulations with 500 random samples and plot the threshold voltage distributions of each device (Fig. 7). Standard deviation (σ_{VT}) and $A_{vt} = \sigma_{VT}\sqrt{WL}$ are summarized in Table 4 and compared to equivalent atomistic simulations presented in [17-18].

MASTAR simulations including variability

For each layout, we run 500 random samples to plot the butterfly curves (Fig. 8) on which we can see that bulk layout is strongly impacted by variability, while FDSOI and FinFET are more robust. This observation is proved with the σ_{SNM} extraction (Table 5).

V_{MIN} extraction methodology

V_{MIN} is the minimum value of V_{dd} where the SRAM cell is functional. If we consider that the SNM distribution is Gaussian, with a mean value SNM_{mean} and a standard deviation σ_{SNM}, the probability to obtain a Static Noise Margin equal to SNM is:

$$P(SNM) = \frac{1}{\sigma_{SNM}\sqrt{2\pi}} e^{\frac{-(SNM-SNM_{mean})^2}{2\sigma_{SNM}^2}} \quad (3)$$

In case of SRAM, a fail is due to a SNM<0. So, from (3), the probability to have a bit fail is:

$$P_{bitfails} = \int_{-\infty}^{0} \frac{e^{\frac{-(SNM-SNM_{mean})^2}{2\sigma_{SNM}^2}}}{\sigma_{SNM}\sqrt{2\pi}} dSNM = \frac{1}{2}\left(1 - erf\left(\frac{Z}{\sqrt{2}}\right)\right) \quad (4)$$

Where Z is the so called "Z-score", equal to SNM_{mean}/σ_{SNM}. For a SRAM array fully functional (i.e. no bit fails), we can write:

$$N_{bitfail} = N_{bits}P_{bitfails} < 1 \rightarrow P_{bitfails} < \frac{1}{N_{bits}} \quad (5)$$

Finally reporting (5) in (4), we obtain the expression of the Z-score for a SRAM array fully functional, as a function of its size:

$$Z = \sqrt{2}\, erf^{-1}\left(1 - \frac{2}{N_{bits}}\right) \simeq 5.9 \text{ for } N_{bits} \sim 100Mbits \quad (6)$$

Therefore, the minimum operating voltage V_{MIN} for a 100Mbits SRAM cell is defined as the value of V_{dd} where Z=SNM/σ_{SNM}=5.9. Then, considering that the SNM is proportional to V_{dd} we can write:

$$SNM = \alpha V_{dd} + \beta \quad (7)$$

Where α and β are determined from SNM(V_{dd}) curves on Fig. 6 Then, considering that $\sigma_{SNM}=0.75x\sigma_{Vt}$ (see Fig. 9) and combining the functionality criteria and SNM(V_{dd}) behavior leads to:

$$\frac{SNM}{\sigma_{SNM}} = \frac{(\alpha V_{MIN}+\beta)}{0.75\sigma_{V_T}} = 5.9 \quad \rightarrow \quad V_{MIN} = \frac{(5.9\ 0.75\sigma_{V_T}-\beta)}{\alpha} \quad (8)$$

Finally, we can evaluate V_{MIN} for each structure (Table 5). We can remark the high value of V_{MIN} (1.19V), superior to the nominal V_{dd} (0.8V) for bulk layout, showing that the bulk SRAM cell isn't functional. Concerning FDSOI (V_{MIN}=0.62V) and FinFET (V_{MIN}=0.64V) SRAM cells, we can conclude that their performances are roughly the same.

Conclusion

In this study, we proposed a benchmark of CMOS device architecture in a SRAM environment, including variability, for the 16 nm node. We demonstrated with the extraction of V_{MIN} that bulk structure is too much impacted by variability to provide functional SRAM cell while FDSOI and FinFET present roughly the same performance.

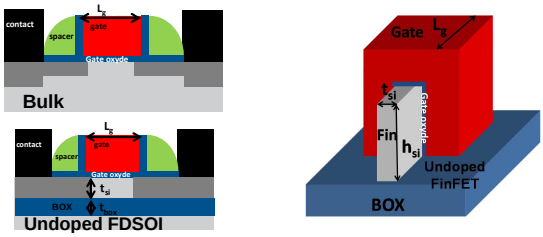

Figure 1: Studied devices, top left: bulk, bottom left undoped FDSOI and right undoped SOI-FinFET

	Equation
C2G	(CPP-L_{nom})/3
L_c	(CPP- L_{nom})/3
W_{ext}	L_{nom}
A2A	(CPP- L_{nom})/3
PS	(CPP- L_{nom})/3
NP	2.(CPP- L_{nom})/3

Table 2: Dimension estimation rules

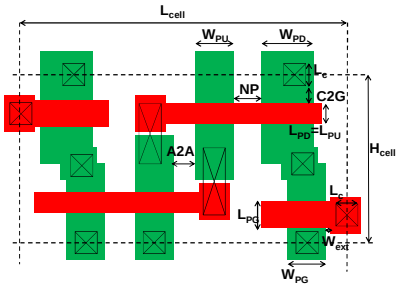

Figure 3: SRAM layout and dimension definition

	BULK	FDSOI	FinFET
W_{PU} (µm)	50	55	60
L_{PU} (µm)	25	20	20
L_{PD} (µm)	25	20	20
W_{PD} (µm)	50	55	60
L_{PG} (µm)	30	26	30
W_{PG} (µm)	42	40	60
SNM (mV)	186	182	186
area (µm²)	0.047	0.046	0.049

Table 3: Layout and area of each SRAM cell.

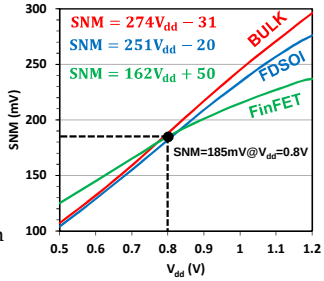

Figure 6: SNM(V_{dd}) curves for each layout. Merger 6 & 8

	BULK	FDSOI	FinFET
σ_L (nm)	0.8	0.8	0.8
σ_{tpm} (mV)	20	20	20
σ_{tsi} (nm)	/	0.2[14]	0.4
σ_{hsi} (nm)	/	/	1
σ_W (nm)	1.6	1.6	1.6
σ_{VT} (mV)	68	30	34
σ_{VT} (mV)	67[17]	/	32[18]
Avt (mV.µm)	2.36	1.04	1.18

Table 4: Process parameter variation distribution .

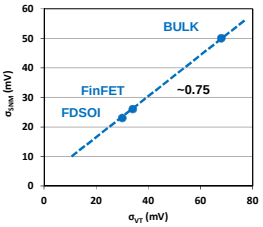

Figure 9: σ_{SNM} vs σ_{VT} for each layout showing that $\sigma_{SNM} \sim 0.75\sigma_{VT}$

	BULK	FDSOI	FINFET
V_{dd} (V)	0.8	0.8	0.8
σ_{Vt} (V)	68	30	34
A_{VT} (mV.µm)	2.4	1.03	1.18
SNM (V)	185.5	182	186
σ_{SNM} (mV)	50	23	26
Area (µm²)	0.0473	0.0464	0.049
V_{MIN} (V)	1.19	0.62	0.64

Table 5: SRAM simulations summary

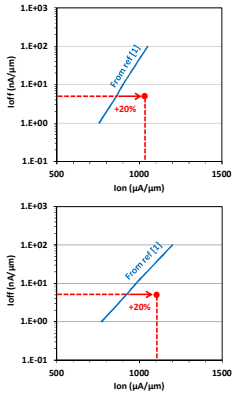

Figure 2: Performance target definition

	BULK		FDSOI		FinFET	
Type	N	P	N	P	N	P
CPP (nm)	64		64		64	
L_{nom} (nm)	20		20		20	
t_{inv} (nm)	1.2		1.2		1.2	
N_{ch} (cm³)	6.8e18		1e16		1e16	
T_{si}/X_j (nm)	10		5		10	
H_{si} (nm)	/		/		25	
t_{box} (nm)	/		10		/	
V_{dd} (V)	0.8		0.8		0.8	
I_{on} (µA/µm)	1080	1050	1100	1078	1128	1115
I_{off} (nA/µm)	124	28	5.0	5.3	5.3	5.4
I_{eff} (µA/µm)	508	465	527	510	564	540
DIBL (mV)	140	140	80	80	68	68
SS (mV/dec)	100	97	80	80	78	78

Table 1: Device geometry and performance

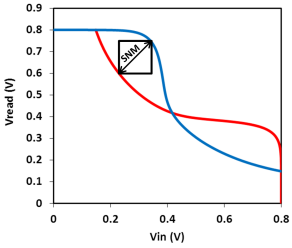

Figure 4: SNM definition.

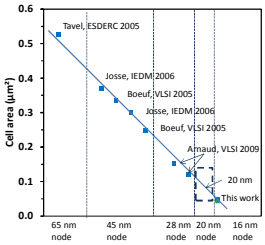

Figure 5: SRAM cell area evolution.

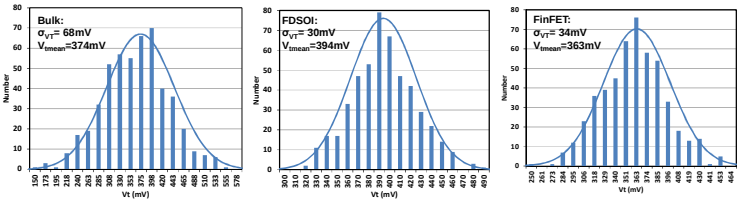

Figure 7: Threshold voltage distribution for each device

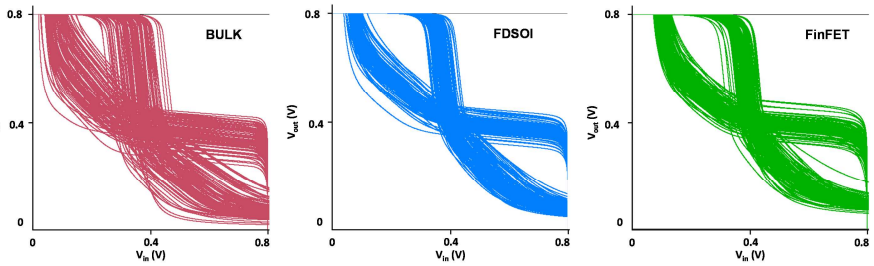

Figure 8: Butterfly curves of each layout at V_{dd}=0.8V

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