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Optimization of 14-nm Node Bulk/SOI FinFETs for SoC Platform: Thermal Conductivity, Operation Temperature, and Analog Performance Analysis

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Introduction

FinFETs have attracted growing interests because of their superior electrostatics. Recently the mass-production of the 22-nm technology node was launched [1]. On the other hand, it is reported that the device temperatures of FinFETs are increased due to the self-heating effect (SHE) [2, 3]. In the previous reports, the thermal conductivity of silicon (λ_{Si}) was assumed to be independent of temperature or equal to the bulk Si value. In addition, SHEs were evaluated under a high DC bias, which may overestimate device temperatures. Therefore, SHEs should be evaluated under a practical bias condition for devices in operations. Although analog performances are important for a system-on-a-chip (SoC) platform, the impact of SHEs on analog performances has not been studied for nanoscale FinFETs.

In this work, the device temperatures and analog performances of 14-nm node Bulk/SOI FinFETs are investigated with a realistic λ_{Si}, for the first time. It is demonstrated that ultrathin-BOX (UT-BOX) SOI FinFETs have a great thermal advantage, because the λ_{Si} size effects result in higher temperature of Bulk FinFETs. It is also shown that analog performances of SOI FinFETs are maximized when BOX thickness (t_{BOX}) is optimized in terms of thermal and electrical properties.

Device Structures & Equivalent Thermal Circuit

Lattice temperature (T_L) and electrical characteristics are calculated using the device simulator by Synopsys Inc. [4]. Table 1 shows the parameters used in the calculations. The parameters are tuned to satisfy the requirements for 14-nm node [5]. In Bulk FinFETs, the thin Si region under the device is *p*+ doped in order to suppress short channel effects [2].

For T_L calculations, the heat dissipation paths from the device to the outside must be defined. In a typical circuit, the drain and gate are connected to the gate and drain of adjacent devices, respectively (Fig. 1(a)). Because the adjacent devices are also operated and the interface thermal resistance reduces the heat flow through the gate [2], the source is the dominant heat dissipation path through interconnects. The thermal resistance of the source interconnect (R_{th}^{int}) is estimated from the approximate expression [6], where the reduced thermal conductivity of Cu (λ_{int}) [7] is incorporated. The thermal resistance (R_{th}) is extracted from the input power normalized by the fin pitch, P ($W \cdot \mu m^{-1}$), and the temperature difference between the channel and substrate ($T_{ch} - T_{sub}$): $R_{th} \equiv (T_{ch} - T_{sub})/P$. R_{th} is consisting of the thermal resistances of the device (R_{th}^{dev}) and R_{th}^{int} connected in parallel (Fig.1 (b)).

Impacts of Reduced Thermal Conductivity

In a heavily doped or thin layer silicon, λ_{Si} is significantly reduced due to a decrease in the phonon mean free path. Fig. 2 shows calculated λ_{Si} of bulk, *n*+ doped, and 7-nm thick (equal to the fin width: W_{fin}) silicon [8, 9]. λ_{Si} is greatly reduced: 60% in *n*+ doped and 90% in 7-nm thick silicon at 300 K, clearly indicating that λ_{Si} should be corrected in nanoscale devices. The *n*+ doped λ_{Si} is applied in the source/drain and gate regions, and the thin layer λ_{Si} is applied in the channel, extension, and thin Si under the channel (for Bulk FinFETs) regions.

The λ_{Si} correction has greater impacts on the thermal properties of Bulk FinFETs, where the generated heat dissipates through the thin Si region. By incorporating the λ_{Si} correction, R_{th} of Bulk FinFETs significantly increases, leading to the thermal advantage of SOI FinFETs when $t_{BOX} < 50$ nm (Fig. 3). In addition, the R_{th} of Bulk FinFETs has the stronger W_{fin} dependence than that of SOI FinFETs (Fig. 4). Since λ_{Si} is getting worse in thinner W_{fin}, the λ_{Si} size effects enhance the W_{fin} dependence of R_{th} in Bulk FinFETs. Therefore, SOI FinFETs also have an advantage from the viewpoint of thermal variability due to the W_{fin} fluctuation (δW_{fin}).

The severe SHE on Bulk FinFETs leads to the drain current (I_d) degradation at a higher gate voltage (V_g) and drain voltage (V_d) region (Fig. 5). However, such a high DC bias around the power supply voltage ($V_g \approx V_d \approx V_{dd} = 0.75$ V) is not applied in a practical circuit operation. In order to evaluate device temperatures in a practical condition, T_L is calculated under a DC bias for analog operations. The bias point is set to be around $V_g = 0.5$ V and $V_d = 0.3$ V. Even under the practical DC bias, the T_L of Bulk FinFETs is significantly higher than that of UT-BOX SOI FinFETs with extremely thin BOX of 5 nm (Fig. 6).

Analog Performance Optimization

Analog performances are analyzed in terms of the cutoff frequency (f_T) and maximum oscillation frequency (f_{max}). f_T and f_{max} are extracted from the h_{21} parameter and Mason's unilateral power gain [10], respectively. Fig. 7 shows f_T/f_{max} as a function of V_d. f_T of UT-BOX SOI FinFETs is higher than that of Bulk FinFETs, thanks to the lower T_L as well as the higher transconductance (g_m) in UT-BOX SOI FinFETs. As V_d increases, the f_T difference between Bulk and UT-BOX SOI FinFETs increases due to the greater SHE in the higher V_d region.

In order to investigate the SHE impacts on analog performances in detail, the t_{BOX} dependences of f_T/f_{max} are evaluated. It is clearly observed that f_T and f_{max} of SOI FinFETs mark the peak at t_{BOX} of 10 and 20 nm, respectively (Fig. 8). As t_{BOX} increases, R_{th} increases (Fig. 3). On the other hand, as t_{BOX} decreases, the parasitic capacitance between the device and substrate (C_{para}) increases. Since the both of R_{th} and C_{para} degrade f_T/f_{max}, f_T/f_{max} are maximized at a certain t_{BOX}. The stronger t_{BOX} dependence of f_T in the thicker t_{BOX} region implies that more serious SHE impacts on f_T.

Conclusions

The impacts of self-heating effects on a practical performance of Bulk/SOI FinFETs are investigated in terms of analog operation with the realistic λ_{Si} for the first time. Fig. 9 summarizes the thermal properties of 14-nm node Bulk/SOI FinFETs. In Bulk FinFETs, we observe higher R_{th}, higher T_L, and greater δW_{fin} impacts on R_{th}. These are mainly due to the λ_{Si} size effects on the dominant heat flow path (thin Si regions below devices). In ultrathin-BOX SOI FinFETs, R_{th} is lower than that of Bulk FinFETs when $t_{BOX} < 50$ nm. f_T/f_{max} take maximum values when t_{BOX} is optimized in terms of thermal (R_{th}) and electrical (C_{para}) properties. f_T of UT-BOX SOI FinFETs is 8% higher than that of Bulk FinFETs at the optimized t_{BOX} of 10 nm. The optimization of analog performances is necessary for the device design of a FinFET-based SoC platform.

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Table 1: Device parameters

Power Supply: V_{dd}	0.75 V
Gate Length: L_g	14 nm
Gate Oxide Thickness: t_{ox}	0.85 nm
Fin Width: W_{fin}	$L_g/2$
Fin Height: H_{fin}	$4W_{fin}$
Extension Length: L_{ext}	$L_g/2$
Fin Pitch: L_{pitch}	$2L_g$
STI Thickness (Bulk FinFET): t_{STI}	100 nm
Thermal Conductivity of Interconnects [5]: λ_{int}	67.7 $Wm^{-1}K^{-1}$
Interconnect Width: W_{int}	19 nm
Interconnect Height: H_{int}	38 nm
Oxide Thickness below Interconnects: t_{int}	300 nm

λ_{int}, W_{int}, H_{int}, and t_{int} are used in the calculation of interconnect thermal resistance (R_{th}^{int}).

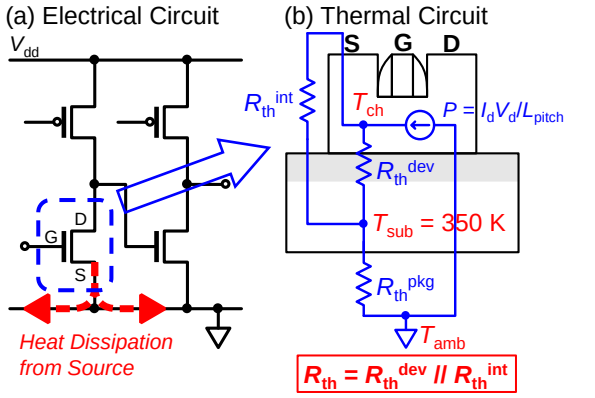

Fig. 1: (a) Heat dissipation paths and (b) equivalent thermal circuit assumed in this work. The source electrode is the dominant heat flow path through interconnects. Thermal resistance (R_{th}) is extracted from temperature difference between the channel and substrate ($T_{ch} - T_{sub}$) with a constant T_{sub} of 350 K. R_{th} is consisting of the thermal resistances of device (R_{th}^{dev}) and interconnect (R_{th}^{int}) connected in parallel. R_{th}^{pkg} and T_{amb} represent thermal resistance of package and ambient temperature, respectively.

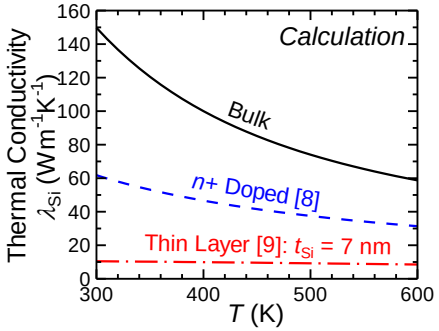

Fig. 2: Thermal conductivity (λ_{Si}) of bulk, n+ doped (phosphorus 1.7×10^{20} cm^{-3}) Si, and 7-nm Si slab as a function of temperature. This figure clearly shows that the conventional bulk λ_{Si} of 148 $Wm^{-1}K^{-1}$ should be corrected for the R_{th} calculation. In heavily doped or thin Si, λ_{Si} degrades significantly due to decreased phonon mean free path.

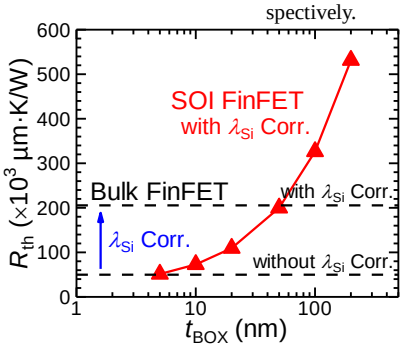

Fig. 3: R_{th} of SOI FinFETs (triangles) vs BOX thickness (t_{BOX}) with λ_{Si} corrections (Fig. 2) and R_{th} of Bulk FinFETs (dashed lines) with and without λ_{Si} corrections. By taking into account the λ_{Si} corrections, it is shown that SOI FinFETs have thermal advantage when t_{BOX} is relatively thick (< 50 nm).

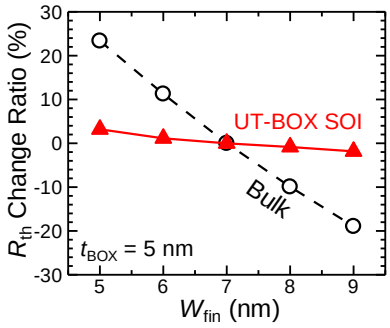

Fig. 4: R_{th} change ratio vs W_{fin} of Bulk and ultrathin-BOX (UT-BOX) SOI FinFETs. Although the variation in W_{fin} (δW_{fin}) strongly affects R_{th} of Bulk FinFETs, R_{th} of SOI FinFETs is almost independent of δW_{fin}.

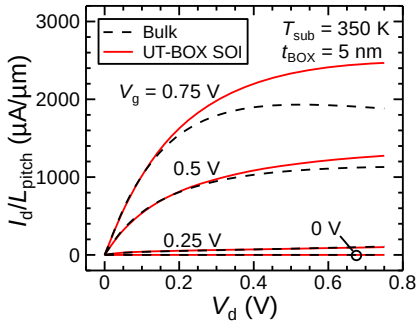

Fig.5: Drain current divided by fin pitch (I_d/L_{pitch}) vs drain voltage (V_d). At higher gate voltage (V_g) and V_d region, I_d/L_{pitch} of Bulk FinFETs is considerably lower than that of UT-BOX SOI FinFETs due to self-heating effect (SHE). The bias point for analog operations is set to be around V_g = 0.5 V and V_d = 0.3 V.

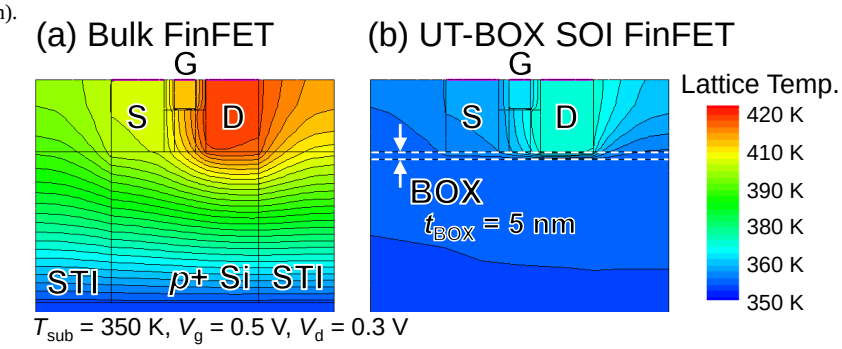

Fig. 6: Contour plots of lattice temperature (T_L) for (a) Bulk and (b) UT-BOX SOI FinFETs under analog operation (V_g = 0.5 V and V_d = 0.3 V). Even under the practical bias conditions for analog operation, the impact of SHE is prominent; T_L of Bulk FinFETs is higher than that of UT-BOX SOI FinFETs.

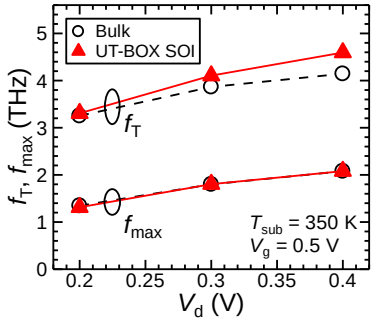

Fig. 7: Cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) vs V_d. f_T of UT-BOX SOI FinFETs is higher than that of Bulk FinFETs. As V_d increases, f_T/f_{max} and f_T difference between Bulk and UT-BOX SOI FinFETs slightly increase.

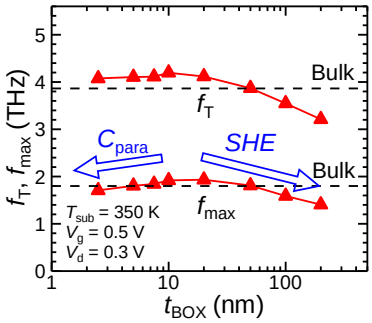

Fig. 8: f_T/f_{max} of SOI FinFETs (triangles) vs t_{BOX}. f_T/f_{max} of Bulk FinFETs are also shown (dashed lines). f_T/f_{max} of SOI FinFETs marked the peak around t_{BOX} = 10 nm. This is because parasitic capacitance (C_{para}) degrades f_T/f_{max} at the extremely thin BOX of 5 nm, whereas thick BOX increases device temperature and degrades transconductance.

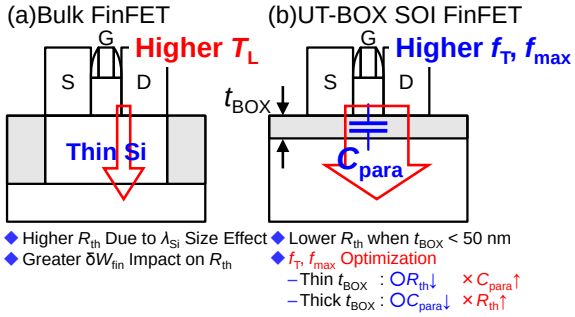

Fig. 9: Schematics summarizing the thermal properties of 14-nm node (a) Bulk and (b) UT-BOX SOI FinFETs. In Bulk FinFETs, higher R_{th} and greater δW_{fin} impact on R_{th} are observed, mainly due to λ_{Si} size effects on the dominant heat flow path (thin Si region below devices). In UT-BOX SOI FinFETs, R_{th} is lower than that of Bulk FinFETs when t_{BOX} < 50 nm. f_T/f_{max} take maximum values when t_{BOX} is optimized in terms of thermal (R_{th}) and electrical (C_{para}) properties. f_T of UT-BOX SOI FinFETs is 8% higher than that of Bulk FinFETs at optimized t_{BOX} of 10 nm.