Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials, Kyoto, 2012, pp825-826

Comprehensive Understandings on Reliability Modulations in Compressive Stressed (100)- and (110)-Orientated Silicon CMOSFETs

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1. Abstract:

Compressive stress impacts on reliabilities in both (100)- and (110)-orientated CMOSFETs were studied systematically. It was interesting to found that, longitudinal compressive stress helps to obtain better NBTI performance in both (100) and (110) pMOSFETs. Also, along with transverse compressive stress increasing in narrow pMOSFETs, better NBTI performance can also be obtained in (110) pMOSFETs, though NBTI degradations was observed in (100) pMOSFETs due to worse STI edges. Furthermore, together with SILC and TDDB characterizations, it is concluded that compressive stress can modulate dielectric/channel interface states and achieve better NBTI performances, while it weakly affects bulk dielectric properties. Underlying physical mechanisms are discussed.

2. Introductions:

Along with CMOS scaling down technologies, reliability in stress-engineered devices attracts more and more attentions. It is known that better initial interface qualities can be obtained by dangling bonds passivation [1], while excessive hydrogen will degrade dielectric reliability on the contrary, as reported in pMOSFETs with compressive SiN film as contact etch stopper layer (CESL) [2]. Also, it was observed that, with CESL compressive stress films, reliability can be improved in both n- and pMOSFETs [3]. So far, stress effects on reliability are mainly studied in MOSFETs with additional stress films or mechanical stressors, but reliability dependence on intrinsic stress, such as layout-induced stress, are easily screened.

In this work, in order to decouple intrinsic stress effects from additional stress film effects screening, both (100) and (110) CMOSFETs are studied and compared, by utilizing layout-induced compressive stress. For further understandings, carrier mobility, NBTI, SILC and TDDB are characterized and compared and discussed. It is interesting to found that, though bulk dielectric properties weakly dependents on compressive stress, better NBTI properties were observed in compressively stressed (100) and (110) pMOSFETs.

3. Measurement Results and Discussions:

Firstly, carrier mobility was characterized to confirm layout induced stress effects [4]. Fig. 1 is layout of studied MOSFETs and TEM images in wide and narrow MOSFETs. Figs.2 and 3 shows measured mobility in (100) and (110) MOSFETs with dependence on L_g and W_g, respectively. In (100) MOSFETs, mobility degradation in short and narrow nMOSFETs are larger than that in pMOSFETs. Comparisons between devices of various X_g were shown in Fig.4. On (100) surface, smaller X_g causes hole mobility enhancements but electron mobility degradations. Mobility modulations strongly indicate the existence of compress stress [4]. In other words, devices with short L_g but same X_g accept stronger longitudinal compressive stress due to smaller active area lengths L_g+2X_g. Observed carrier mobility modulations in Figs.2~4 can be explained well by considering layout-induced compressive stress. Also, gate leakage (J_g) modulations were measured. Due to compressive stress effects [5-6], J_g increases in (110) nMOSFETs of smaller X_g while decreases in pMOSFETs. Measured V_{th}, J_g and μ_{eff} are summarized in Table I for reference. Then, interface states were characterized by using charge-pumping (CP) method. Based on extracted W_g dependence of I_{cp} in Fig. 5, it is found that, D_{it} at (100) interface has large degradations as shrinking W_g, which can be explained by larger contributions from worse STI edge [7]. However, D_{it} at (110) interface has weak W_g dependence due to originally worse Si/SiO_2 interface.

Next, reliability properties were characterized systematically. As shown in Fig. 6, in (100) pMOSFETs, worse NBTI is observed in narrow channel devices, which agrees with worse D_{it} (Fig.5). However, NBTI is surprisingly improved in narrow (110) pMOSFETs. Opposite W_g dependence on (100) and (110) pMOSFETs can be clearly distinguished in Fig. 7. Then, NBTI are measured in devices of various X_g. As longitudinal compressive stress increases with X_g shrinking, better NBTI are observed in both (100) and (110) pMOSFETs (Fig. 8), indicating that better NBTI originates from larger compressive stress. Stress induced leakage current (SILC) is characterized in devices of various designs to study stress effects on bulk dielectric properties, as shown in Fig. 9, however, there is no obvious difference in all studied devices. Time dependent dielectric breakdown (TDDB) properties are measured in rectangular capacitors of 1um and 0.5um side length. Similarly, there is no difference in Weibull distributions (Fig. 10). In summary, layout-induced stress results in improved NBTI but has weak effects on the quality of bulk dielectrics (Fig. 11).

It deserves to be noted here, different from previous work [1-3], there is no additional stress film in studied devices and proposed CESL stressing layer impacts in [3] can not explain observed better NBTI performance in this work. Nevertheless, since compressive stress from shrinking gate-to-STI distances previously existed before gate oxidation, it is believed that interface states creations during gate oxidation can be affected by initially existed surface stress states [8]. Also, according to two stage model in [9], Si-Si at SiO_2 side should break before Si-H breaking. Thus, though initial states are almost identical, Si-H at stressed Si/SiO_2 interface is difficult to break due to stronger Si-Si bonding, and less Si-H breaking results in better NBTI performances.

4. Conclusions:

Systematical investigations were done for comprehensive understandings on layout-induced stress effects in CMOSFETs reliability. It is interesting to found that, in both (100) and (110) pMOSFETs, longitudinal compressive stress results in better NBTI. However, with stronger transverse compressive stress, better NBTI can be only obtained in (110) pMOSFETs, but NBTI degradations were observed in (100) pMOSFETs due to worse STI edge impacts. Also, layout induced stress has weak effects on SILC and TDDB performances. Suppressed Si-H breaking at compressively stressed interface is considered to explain observed phenomena. This work indicates that stress engineering, as both performance and reliability booster, is an important candidate for future CMOS technology.

References:
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[4] M. Saitoh *et al.*, IEDM, 2008, p573;
[5] S.E. Thompson *et al.*, TED, 53(5), 2006, p1010;
[6] M. Saitoh *et al.*, VLSI, 2008, p.18;
[7] H. Lee *et al.*, TED, 49(4), p605, 2002;
[8] P. Somers, et al. JAP, 103, p033703, 2008;
[9] T. Grasser, *et al.*, IRPS, 2009, p33.

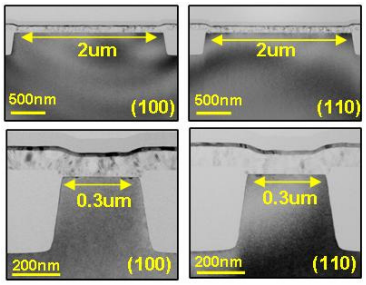

Fig.1 TEM images of transverse cross sections in (100) and (110) MOSFETs of 2um and 0.3um W_g.

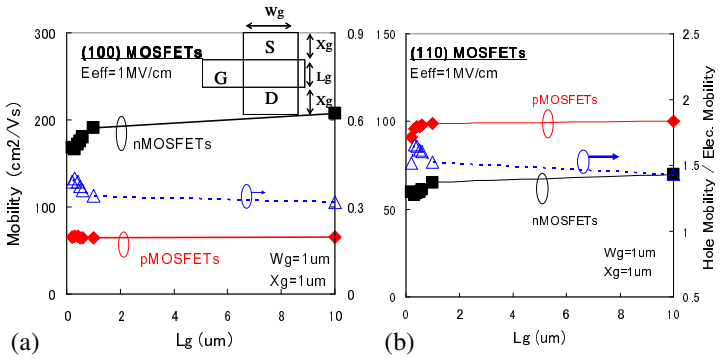

Fig.2 Mobility in (a) (100)/<110> and (b) (110)/<110> MOSFETs of various L_g. Mobility degradation in short and narrow nFETs and pFETs except in (100) pFETs.

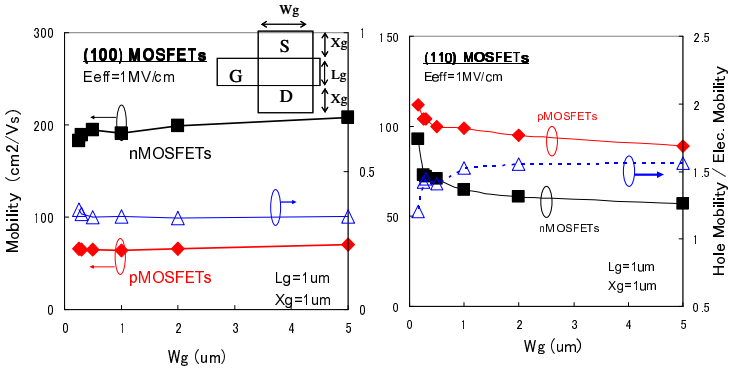

Fig.3 Mobility in (a) (100)/<110> and (b) (110)/<110> MOSFETs of various W_g. Mobility enhancements in short and narrow nFETs are observed in (110) nFETs and pFETs.

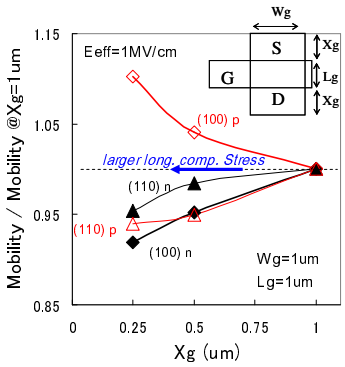

Fig.4 Mobility modulations in n-/p- FETs as shrinking X_g.

	@ Xg Scaling (*long. stress*)		@ Wg Scaling (*trans. stress*)	
Type	Jg	μeff	Jg	μeff
(100) nFETs	↑	↓	↑	↓
(100) pFETs	↓	↑	↓	↓
(110) nFETs	↑	↓	↑	↑
(110) pFETs	↓	↓	↓	↑

Table I Summary of modulations of J_g, and μ_{eff} with X_g and W_g scaling

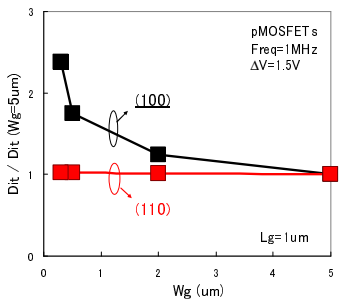

Fig.5 Comparisons of W_g dependence of I_{cp} in (100) and (110) pMOSFETs. In (110) pFETs, I_{cp} modulations are negligible.

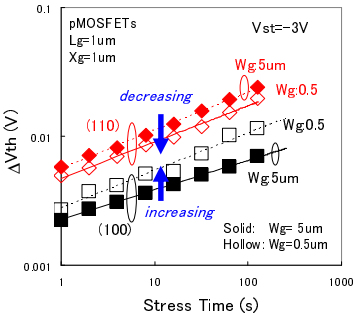

Fig.6 NBTI in 5um and 0.5um W_g pFETs. NBTI is improved in narrow (110) pFETs from wide (110) pFETs.

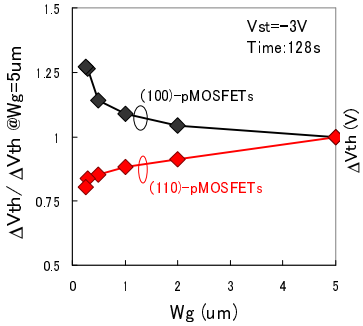

Fig.7 W_g dependence of NBTI properties. As shrinking W_g, NBTI improves in (110) pFETs while degrades in (100) pFETs.

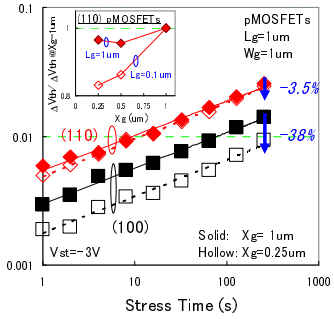

Fig.8 NBTI characteristics in pFETs of 1um and 0.25um X_g. NBTI are improved in pFETs of small X_g.

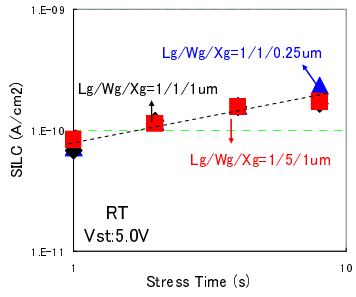

Fig.9 SILC properties in devices of various W_g and X_g. Similar SILC properties are observed in all devices

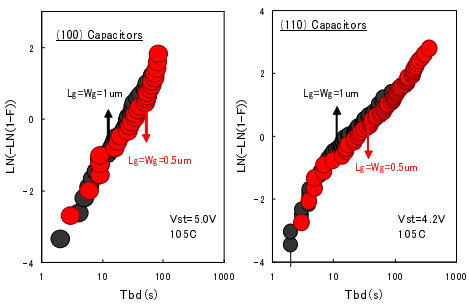

Fig.10 TDDB characterizations in 1um and 0.5um $L_g(W_g)$ capacitors, (a) (100) and (b) (110) capacitors.

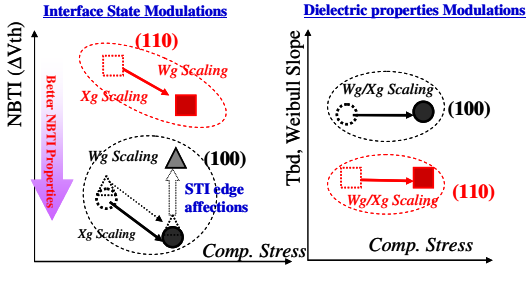

Fig.11 Summary of NBTI and TDDB characteristics modulations in MOSFETs of various designs, indicating that compressive stress is effective to improve interface properties.