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Characterization and Modeling of Back Bias Impacts on Remote-Coulomb-Limited Mobility in UTBB-FDSOI Devices

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1. Introduction

Ultra Thin Box and Body Fully Depleted SOI device (UTBB-FDSOI) is a good candidate to come after the conventional planar bulk technology [1-3]. Among the benefits offered by such structures, it has been shown that applying a positive Back Bias (BB) can significantly change the threshold voltage and thus boost the performances or alternatively reduce the power consumption of a system [1-2]. Recently, additional electron mobility enhancement has been reported when BB is applied in forward regime (VB>0 for NMOS and VB<0 for PMOS) [3]. Direct comparison and temperature measurements of the front- and the back-interface mobility of devices are provided in [4].

This paper presents a thorough study of both electrostatics and effective channel mobility in a large range of back bias (up to 10V). We focus on Metal Gate NMOSFETs featuring 1.8nm High-K oxide on top of 1.13nm single Oxide (GO1) and 4nm double Oxide (GO2) interfacial SiO_2 layer, for respectively high performance and low power application.

2. Experiments

Figures 1 and 2 demonstrate respectively the impact of the BB on the Drain current and on the capacitance for both devices. As can be seen, the threshold voltage can be significantly adjusted changing VB (Figure 3). It is worth noticing that the sub-threshold slope is nearly unchanged (less than 7%; not shown). Figure 4 shows the GO1 device effective channel mobility. At zero BB, the mobility is relatively low (≤ 200 cm^2/V/s) which is usual in High-K Metal gate devices [5-10]. As recently shown [3], the mobility can be significantly changed when a positive BB is applied. Similar extractions in the GO2 device are shown in Figure 5. In that case, the applied BB voltage range is larger (VB=-10V up to 10V) and a smooth and non-monotonic mobility behaviour is clearly noticeable for VB>0V. In contrast with Remote Coulomb (RC) effects on the mobility (mostly visible at low inversion charge), we will demonstrate that this unusual behaviour is a direct consequence of back channel inversion occurring at large BB.

3. Mobility and Effective field

In the following, we present Kubo-Greenwood-based (KG) simulations accounting for phonon scattering, screened SiO2/Si Roughness and RC-scattering [5-10]. The device electrostatic and the KG ingredients (wave functions, energy levels) are obtained from a Poisson-Schrodinger solver [11]. An accurate calibration of the devices geometry (front gate High-K/SiO2 thicknesses but also buried oxide and channel thicknesses) is mandatory in order to account for the observed C-V and mobility vs. BB. This is shown in Figure 6 where the capacitance is simulated for two channel thicknesses (T_{Si}=5.5nm and T_{Si}=7.5nm). The change in capacitance shape for positive BB is well known (also visible in Figures 2 and 3) and can be inferred from the intrinsic channel capacitance C_{Si} in series with the oxide one C_{ox} [1].

Figure 7 shows the simulated mobility at zero BB for both devices. Large charges density at High-K/SiO2 interface has been introduced to match experimental data (e.g. in the GO1 device N_{it}~6.3e^{12} /cm^2). Several other mechanisms, such as Optical Soft phonons (SOph), High-K/SiO2 Interface Roughness [9] and neutral defects [7,11] in the near-Source/Drain regions have been suspected to be at the origin of the observed mobility degradation in High-K Metal Gate MOSFETs. However, recent studies [1, 2] have highlighted that, in devices with thick SiO2 interfacial layer (T_{IL}>1nm), SOph scattering shows a smaller influence on carrier mobility than originally suspected, and are neglected. In the GO1 device additional contributions have been added to the mobility to account for the influence of neutral defects and High-K/SiO2 interface roughness [7,9,11].

Figures 8 show mobility curves as a function of effective field [12] approximated with:

$$E_{eff}^{exp} = \frac{C_{ox}}{2\varepsilon_{SI}}(VG + V_{TH}) + cst \qquad \text{(eq1)}$$

Also shown are the theoretical results with theoretical field:

$$E_{eff}^{theo} = \frac{\int \frac{\partial V(z)}{\partial z} n(z)dz}{\int n(z)dz} \qquad \text{(eq2)}$$

As can be seen, the experimental and the theoretical mobility curves follow a unique trend and the apparent mobility improvement shown in Figure 4 is related to a change of E_{eff} vs. BB.

4. Discussion

To go further, we now discuss the mobility in the GO2 device shown in Figure 9. We notice that E_{eff} (also shown in Figure 10) can be negative and in particular for large positive BB. In this case, back interface is inverted as depicted in Figure 11 where band diagrams are extracted for $|E_{eff}|$~0.65MV/cm at either VB=0 or VB=8V. A clear displacement of the inversion charge (shown in Figure 11 c)) toward the back Oxide interface occurs in the latter case. Corresponding mobility, shown in Figure 9, decreases nearly symmetrically for E_{eff} negative and positive values.

Both front and back interfaces with the SOI thin films are made of thermally grown oxide which is in live with the nearly identical mobility noticed here, and indicates that in the strong inversion regime the mechanisms limiting the mobility are rather similar (due to a partial or total screening of the RC effects). This contrasts with the ~50% gain in back gate mobility vs. front gate mobility measured in High K/ Si FDSOI devices reported in [4]. We believe that, in our GO2 device, the presence of the thick oxide interfacial layer significantly reduce the trap density at the top Si interface. Further results obtained in PFDSOI devices supporting these observations will be shown and discussed at the conference.

5. Conclusion

FDSOI devices with ultra thin BOX make possible versatile characterization of the front and back gate mobility. Experimental results and simulations evidence a clear inversion of the back interface when positive BB is applied, which makes possible a *direct* comparison between the physical mechanisms responsible of the mobility degradation at the High-K/ SiO2 front interface and at the SiO_2 back interface.

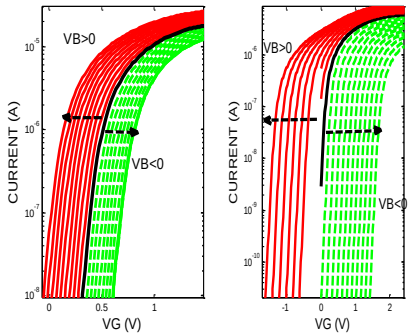

Figure 1 : Drain Current as a function of Gate voltage (VG) for various Back Bias voltages ranging from -5V to 5V in the GO1 NFDSOI (left) and from -10V to 10V in the GO2 NFDSOI (right); WxL=0.9µmx9µm.

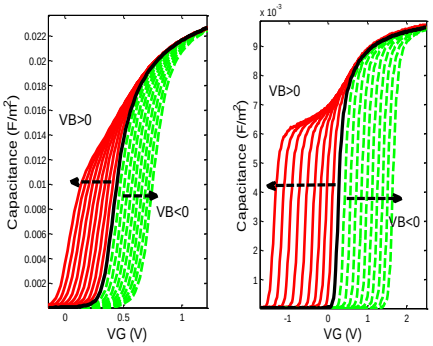

Figure 2 : Gate capacitance measured in the same devices as in Fig. 1.

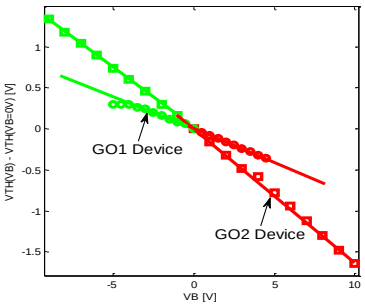

Figure 3 : Extracted Threshold voltage variation in GO1 and GO2 NFDSOI. Lines are guides for the eyes.

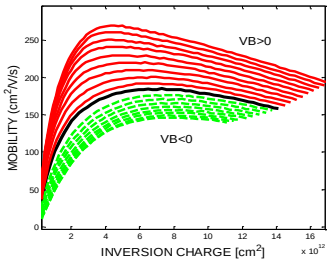

Figure 4 : Effective mobility as a function of the inversion charge extracted for VB (from -5V to 5V) in the GO1 NFDSOI.

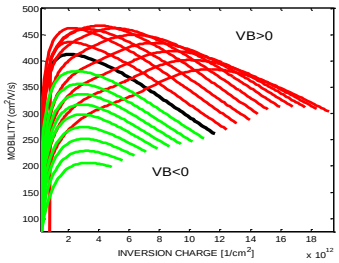

Figure 5 : Effective mobility as a function of the inversion charge extracted for VB (from -10V to 10V) in the GO2 NFDSOI. An unusual behavior can be observed for positive BB.

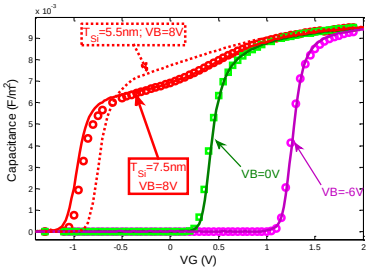

Figure 6 : GO2 NFDSOI simulated capacitance (symbols) as a function of Gate voltage compared to measurements (solid lines). Also shown, are simulations (dashed lines) for VB=8V for the same device but with T_{SI}=5.5nm.

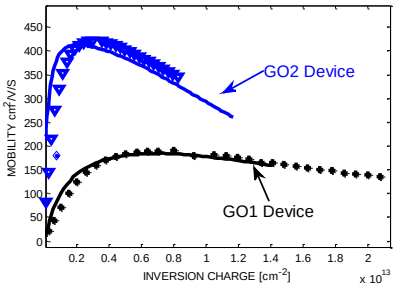

Figure 7 : Calibrated mobility at zero Back Bias. Lines: measurements and symbols: simulations.

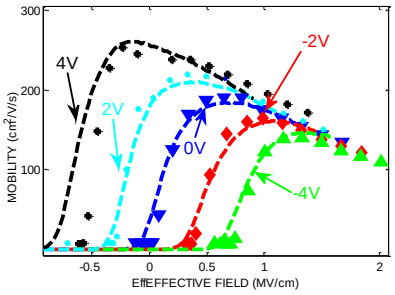

Figure 8 : Effective mobility as a function of the channel effective field in GO1 FDSOI NMOSFET. From left to right; VB=4V, 2V, 0V, -2V, and -4V. Symbols: simulations; lines: experiments.

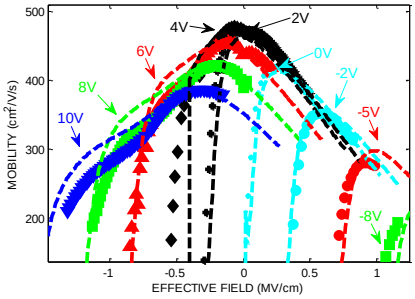

Figure 9 : Same as for Fig. 8 but for GO2 NFDSOI. From left to right; VB=10V, 8V, 6V, 4V, 2V, 0V, -2V, -5V and -8V.

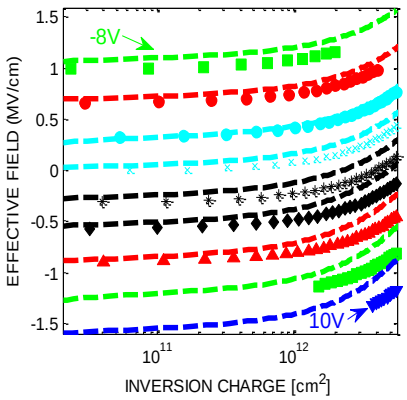

Figure 10 : Effective field as a function of inversion charge density. Theoretical results (Symbols) obtained with eq 2 and experiental results (lines) with eq. 1. From bottom to top; VB=10V, 8V, 6V, 4V, 2V, 0V, -2V, -5V and -8V.

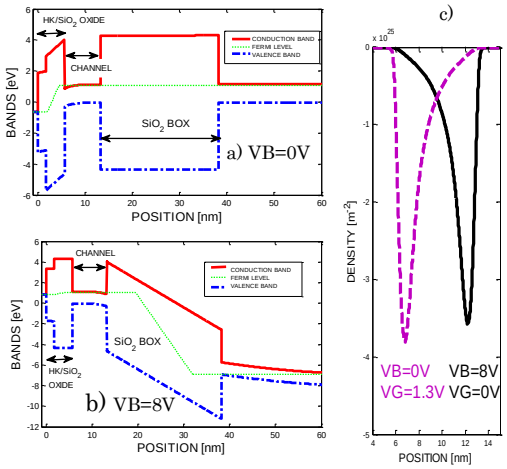

Figure 11 : Band Diagrams of the GO2 FDSOI device when (a) the Back terminal is ungrounded and (b) with a 8V Back bias. The effective channel field is +0.652 MV/cm and -0.65MV/cm respectively. The inversion charges are shown in c).

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