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Novel Extraction Method for Source and Drain Series Resistances in Silicon Nanowire MOSFETs Based on Radio-Frequency Analysis

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1. Introduction

The source and drain (S/D) series resistances become critical parameters to model MOSFET characteristics based on nanowire structure. Although S/D series-resistance extraction methods based on a small-signal radio-frequency (RF) analysis have been reported, only planar structure with substrate components [1-3] or off-state bias-independent components [1, 4] have been considered.

In this paper, we propose a novel extraction method for S/D resistances of silicon nanowire (SNW) MOSFETs in consideration of bias-dependent RF components from both *Y*- and *Z*-parameters. The extraction results by our proposed method for the SNW MOSFETs are compared with those by the previous work [2]. The Y_{22}- and Z_{22}-parameters generated by HSPICE [5] showed good agreements with those obtained from three-dimensional (3-D) device simulation up to 100 GHz [6].

2. RF Model and Extraction Method

Figure 1 shows an equivalent circuit of an SNW MOSFET device operating in the strong inversion region ($V_{GS} > V_{th}$) with V_{DS} = 0 V, which results in the negligible transconductance (g_m) [3]. In this equivalent circuit, C_{gs} and C_{gd} are the intrinsic gate-to-source and gate-to-drain capacitance, respectively. Also, C_{gse} and C_{gde} are the extrinsic gate-to-source and gate-to-drain capacitance, respectively. The resistance components of R_{elect} and R_{ch} are the gate electrode resistance and the channel resistance, respectively. In terms of the S/D resistance, R_{si} and R_{di} are the gate bias-dependent S/D series resistances. In addition, R_{se} and R_{de} are the gate bias-independent source and drain series resistances. When the device is turned off, the intrinsic gate capacitances can be ignored and the channel resistance increases infinitely owing to the absence of channel charges. Therefore, the C_{gs}, C_{gd}, R_{ch}, R_{si}, and R_{di} can be removed from the equivalent circuit model in case of an off-state.

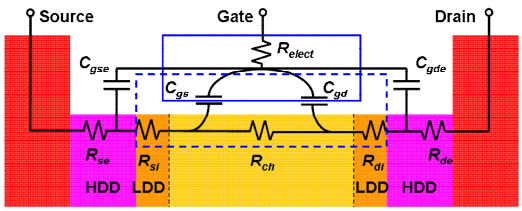

Fig. 1 Equivalent circuit with the cross-sectional view of an SNW MOSFET.

The *Y*-parameters for the simplified equivalent circuit at the turn-off region are derived as following equations:

$$Y_{11} \approx \omega^2\left[R_{elect}\left(C_{gse}+C_{gde}\right)^2+R_{se}C_{gse}^2+R_{de}C_{gde}^2\right] + j\omega\left(C_{gse}+C_{gde}\right) \quad (1)$$

$$Y_{12} \approx -\omega^2\left[R_{elect}C_{gde}\left(C_{gse}+C_{gde}\right)+R_{de}C_{gde}^2\right]-j\omega C_{gde} \quad (2)$$

$$Y_{22} \approx \omega^2\left(R_{elect}+R_{de}\right)C_{gde}^2+j\omega C_{gde} \quad (3)$$

The capacitances are obtained from the imaginary parts of *Y*-parameters. Also, the equations for the resistance-related components extraction are provided as follows:

$$R_{de}=\frac{C_{gde}\,\mathrm{Re}(Y_{12})+\left(C_{gse}+C_{gde}\right)\mathrm{Re}(Y_{22})}{\omega^2 C_{gse}C_{gde}^2} \quad (4)$$

$$R_{elect}=-\frac{\mathrm{Re}(Y_{12})+\omega^2 R_{de}C_{gde}^2}{\omega^2 C_{gse}\left(C_{gse}+C_{gde}\right)} \quad (5)$$

$$R_{se}=\frac{\mathrm{Re}(Y_{11})-\omega^2 R_{elect}\left(C_{gse}+C_{gde}\right)^2-\omega^2 R_{de}C_{gde}^2}{\omega^2 C_{gse}^2} \quad (6)$$

The extrinsic R_{elect}, R_{se}, R_{de}, C_{gse}, and C_{gde} components are independent of gate bias. After de-embedding these values from the small-signal equivalent circuit in Fig. 1(a), the Y_{11}- and Z_{22}- parameters can be derived as follows:

$$Y_{11} \approx \omega^2\left(\frac{R_{si}R_{di}\left(C_{gs}+C_{gd}\right)^2+R_{ch}\left(R_{di}C_{gd}^2+R_{si}C_{gs}^2\right)}{R_{ch}+R_{si}+R_{di}}\right) + j\omega\left(C_{gs}+C_{gd}\right) \quad (7)$$

$$\mathrm{Re}\left(Z_{22}\right)\big|_{\omega^2=0} \approx R_{ch}+R_{si}+R_{di} \quad (8)$$

Since the simulated structure has symmetry about the channel center, R_{si}, R_{di}, and R_{ch} can be extracted by following equations:

$$R_{si}=R_{di}=\mathrm{Re}(Y_{11})/\left(2\omega^2 C_{gs}^2\right) \quad (9)$$

$$R_{ch}=\mathrm{Re}\left(Z_{22}\right)\big|_{\omega^2=0}-\left(R_{si}+R_{di}\right) \quad (10)$$

3. Results and Discussion

In order to extract the small-signal parameters, both *Y*- and *Z*-parameters of SNW MOSFETs up to 100 GHz are obtained from 3-D device simulation [6]. SNW MOSFETs with channel length (L_G) of 30 nm have radius (R_n) of 5 nm and 10 nm. The doping concentration of n-type lightly doped drain (LDD) region and highly doped drain (HDD) region is 5×10^{18} cm^{-3} and 1×10^{20} cm^{-3}, respectively.

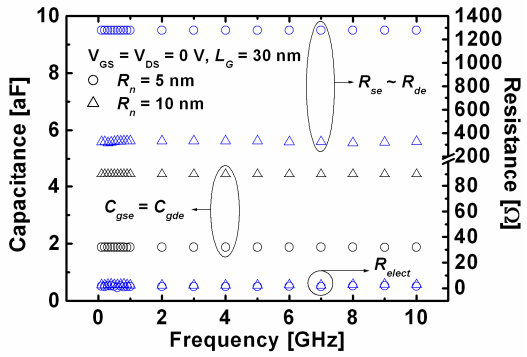

Fig. 2 Small-signal parameters extracted at $V_{GS} = V_{DS} = 0$ V.

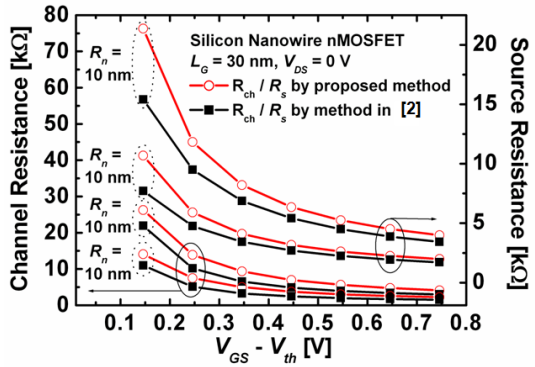

Fig. 3 Resistance components extracted from SNW MOSFETs with different nanowire radius (R_n) at $V_{GS} > V_{th}$ with $V_{DS} = 0$ V.

Figure 2 shows the extracted small-signal parameters as a function of frequency at $V_{GS} = V_{DS} = 0$ V. The extracted parameters remain almost constant with frequency, which validates the reliability of the proposed method. In this simulation work, R_{elect} has been kept as negligibly small by using metal gate electrode. The gate-bias independent source resistances of devices with R_n = 5 nm and 10 nm are 1298.8 Ω and 327.4 Ω, respectively, which proves that the proposed method is still applicable to the extremely scaled MOSFET devices. Fig. 3 shows the extracted total source series resistances ($R_s = R_{si} + R_{se}$) and channel resistances (R_{ch}) as a function of gate overdrive voltage ($V_{GS} - V_{th}$) based on our newly proposed method in comparison with the previous work [2], which always underestimates the nanowire series resistance for all different radius due to substrate components only existing in the planar structure.

In order to evaluate the accuracy of our proposed extraction method for nanowire structure, the Y_{22}- and Z_{22}-parameters from 3-D device simulation results have been compared with those from circuit simulation by HSPICE based on the extracted parameters and the proposed small-signal equivalent circuit in Fig. 1. As shown in Fig. 4, the simulation results from an equivalent circuit based on the new extraction method successfully reproduce the 3-D device simulation results up to near 100-GHz. Parameters extracted by the previous method [2], however, show the significant deviations of HSPICE results from 3-D simulation data.

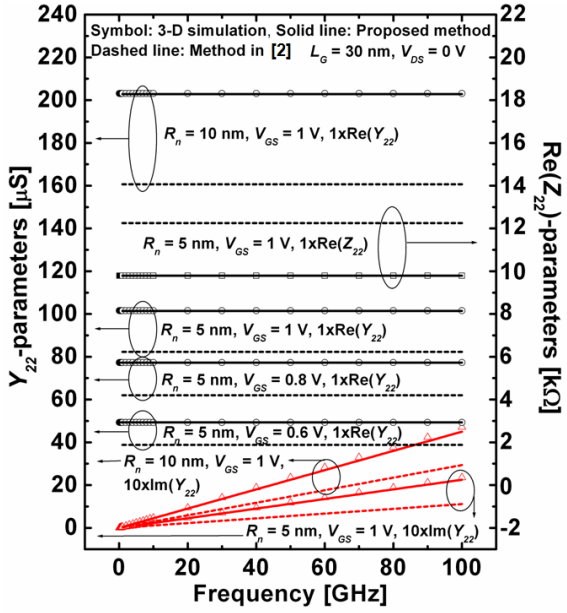

Fig. 4 Comparison of the physical 3-D device simulation data with the schematically modelled Y_{22}-and Z_{22}-parameters for a 30 nm SNW MOSFET device.

As shown in Fig. 4, the frequency-independent output impedance (Re(Z_{22})) and admittance (Re(Y_{22})) from the HSPICE simulations based on our method for nanowire structure without substrate parasitic also demonstrated good consistency with the 3-D device simulation results up to 100-GHz at various gate voltages even in the on-states.

4. Conclusions

An analytical method of extracting S/D series resistance of SNW MOSFETs from the RF parameters has been proposed. Our methodology showed higher accuracy for a nanowire than the previous bias-independent method on planar MOSFETs. The schematically modeled *Y*- and *Z*-parameters have demonstrated excellent agreements with the 3-D simulation results up to 100-GHz range.

Acknowledgements

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