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A Novel and Direct Measurement of the Mobility on Very Small Dimension CMOS Devices with Channel Length Down to 20nm

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Abstract- Mobility is the most fundamental parameter to understand the transport mechanism in advanced CMOS technology. In this work we demonstrated that: (1) a novel and simple CV measurement has been developed to extract mobility from a single device down to 20nm; (2) the strain effects in different device structures can be better understood from these measurements. Results show that the mobility of device indeed increases with the strain effect, while the mobility will be reduced with the further scaling of device dimensions. Our approach provides a total understanding to directly measure the mobility and carrier scattering from a single ultra-scaled device, which provides very practical use for the device design using strain technology and for the study of CMOS scaling.

1. Introduction

Moore's Law has driven CMOS devices scaling for several decades. To further boost the performance, strained-Si technology and ultra-thin gate oxide have been employed in the CMOS devices.[1-2] The most important parameter for high performance design is the channel mobility. However, it has been very difficult to extract the mobility directly from a single small device. Some methodologies have been developed to extract the mobility, including RF split-CV[3] and magnetic Hall mobility[4], but required sophisticated set-up, which revealed certain limitations. In this work, a simple CV measurement has been developed. Fig.1a is the conventional 4-terimanl CV. Fig. 1b is the split CV with 3-terminal. Fig. 1c is our newly developed 2-terminal CV measurement, showing the lowest over-lapped capacitance and less parasitic effect such that the mobility measurement on a very short channel length device becomes feasible. (Fig. 1d) This paper will first demonstrate the method and it will be further extended to study small dimensional strained SiC S/D nMOS with CESL and SiGe S/D pMOS devices.

2. Device Preparation

32nm poly-Si gate CMOS device technology, with SiON insulator, was used in the fabrication of test devices, including the control and strained SiC S/D nMOS devices with CESL [5]; the control and strained SiGe S/D pMOS devices [6]. (Fig.2) The charge pumping technique is utilized to extract the effective gate length, $L_{eff}= L_{mask}-\Delta L$. (Fig.3)

3. Results and Discussion

A. Simple Two-terminal CV Measurement

After an accurate RCL correction, by applying this simple two-terminal CV measurement, the experimental results of channel inversion capacitance are shown for pMOS (Fig. 4a) and nMOS (Fig. 4b), respectively. The zoom-in plot, Fig. 4c, shows an interesting phenomenon, in which CV curves presented a two-slope trend in short channel devices owing to the *halo implant* near the drain (or source), Fig. 4d. As the channel length reduces, the halo impurity in the proximity of channel, causes a two-slope in C-V curves. It is manifested in the local threshold voltage profile from this new CV method which shows a shifted halo implant barrier with the channel lengths. The results from the charge pumping technique, Fig.5, show good matches with the current CV results.

B. Mobility Extraction from a Single Ultra-scaled Device

With the help of experimental CV results, the inversion charges, integrated by CV data (Fig. 6), shows a stronger length dependency in the pMOS devices but not for the nMOS devices because the quantization of ultra-short channel provides more sub-bands and contains more carriers between the heavy- and light-hole bands in pMOS devices. This phenomenon will affect the I_{Dlin} ratio between nMOS and pMOS devices. Fig. 7 shows this ratio approaches to unity as the length reduces because the increase of charge in pMOS devices enhances the I_{Dlin} of pMOS devices although mobility of pMOS devices is much smaller than that of nMOS devices. The experimental results of mobility for CMOS devices with various channel lengths are shown in Fig. 8. Mobilities of strained devices are apparently enhanced, but are reduced with reducing gate length.

C. *More Observations on the Mobility of Strained CMOS Devices*

An experimental parameter, defined as the *surface scattering rate,* $\Delta\mu/\Delta V$, can be used as a monitor of the surface roughness in the mobility of strained devices. The larger this parameter is, the more serious the surface scatting is. Fig. 9 shows that the scattering rate becomes smaller as the length reduces because of the decrease of surface scattering. Fig. 10 shows the mobility enhancement of strained devices, in which, for strained nMOS devices, it decays in the beginning due to the relaxation of CESL strain and then increases afterward owing to the enhancement of uniaxial SiC S/D strain. In comparison, for strained pMOS devices, mobility enhances as channel reduces since the SiGe stressor is much closer to the channel, enhancing the stress and also the mobility. Finally an interesting comparison is shown in Fig. 11, where the delay time of strained nMOS devices (**top**) and pMOS devices(**bottom**) are flattened out, which sets a limit on the further scaling of CMOS devices.

In conclusion, a simple *CV measurement* technique has been demonstrated on CMOS devices with gate length down to 20nm, which is believed to be the shortest length that can be demonstrated in reported-to-date. By applying this approach, several salient features have been achieved: (1) A simple and easy 2-terminal CV has been implemented for a single device mobility measurement, (2) The mobilities of strained devices are apparently enhanced, but are reduced with reducing gate length, and (3) the delay time does not obey the constant EOT model, while our new results show that it flattens out. This sets a certain speed limit to the CMOS devices when the device is further scaled.

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References: [1] K. Rim et al., *VLSI Tech.*, p. 98(2002). [2] K. Mistry et al., *IEDM*, p. 247(2007). [3] E. S. Andres et al, *IEEE EDL* p.772(2006). [4] J. P. Campbell et al., *VLSI Tech.*, p. 75(2010). [5] S. S. Chung et al., *VLSI Tech.*, p. 158(2009). [6] C. H. Tsai et al., *VLSI Tech.*, p. 188(2006).

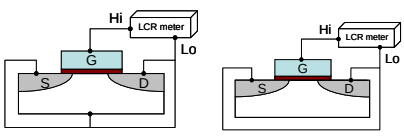


Fig. 1a 4 terminals

Fig. 1b 3 terminals

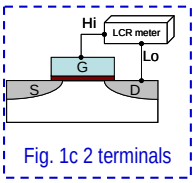


Fig. 1c 2 terminals

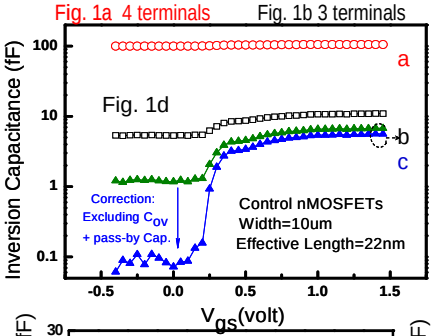


Fig. 1 The CV measurements: (**1a**) 4-terminal CV measurement. (**1b**) 3-terminal CV measurement. (**1c**) **proposed new 2-terminal CV measurement**, (**1d**) The measured results for the above 3 cases from 1a to 1c. Case 1c shows the smallest overlap capacitance and is more reliable than the other 2 cases.

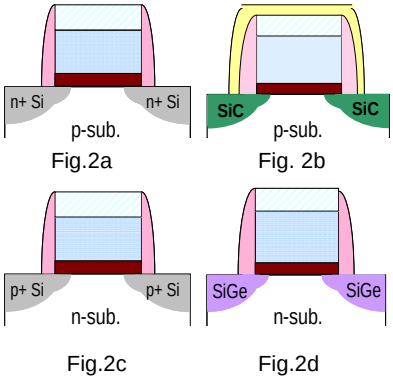


Fig. 2 The cross-section of nMOSFETs: (**2a**) control , (**2b**) SiC S/D devices; pMOSFETs: (**2c**) control , (**2d**) SiGe S/D pMOSFETs.

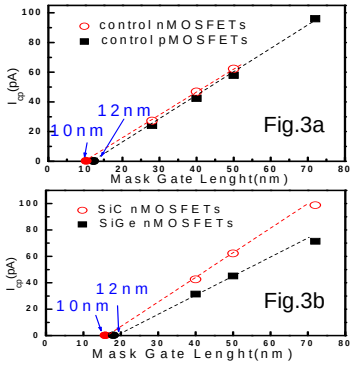
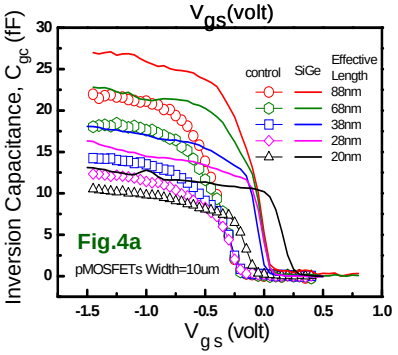
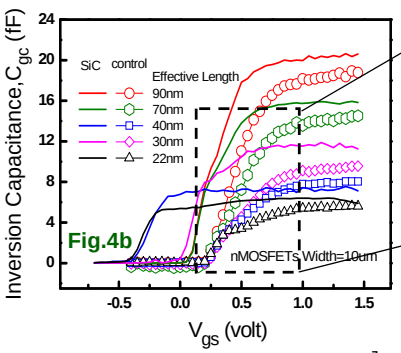
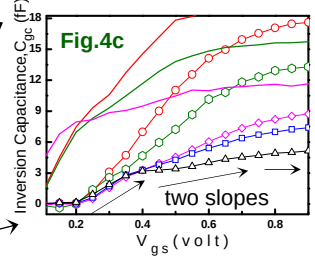


Fig. 3 Extraction of the effective gate length by the CP measurements.







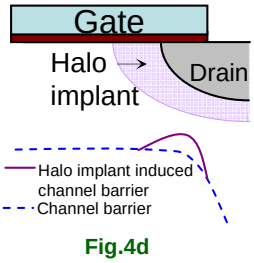
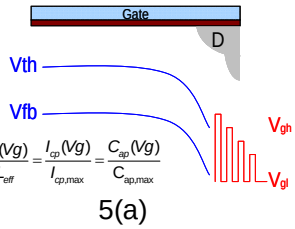


Fig. 4 The experimental results measured by 2-terminal CV for control and strained pMOS(**4a)**; control and strained nMOS(**4b**). The zoom-in (**4c**) shows a two-slope trend in ultra-short channel devices, caused by the heavy **halo implant**. This halo implant induces a higher channel barrier near drain or source side. **New CV technique** has been demonstrated to profile the halo-implant induced channel barrier.(**4d**)



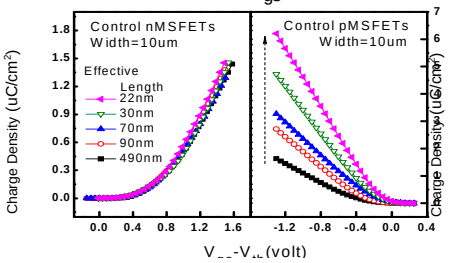


Fig. 6 The charge density of control nMOSFETs (***left***) and pMOSFETs (***right***). Note that the charge density of pMOSFETs increases largely with reducing channel length.

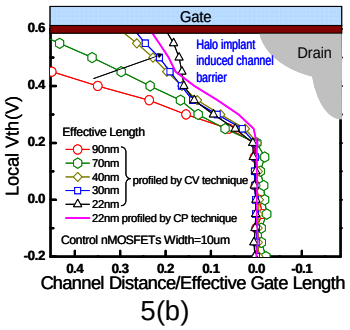


Fig. 5 (a) **A new CV profiling technique** used to profile the halo-implant induced barrier, and (b) the comparison of results with charge pumping profiling results.

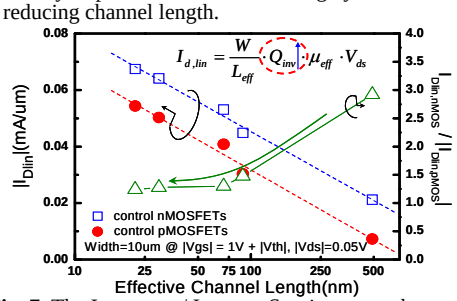


Fig. 7 The IDlin,nMOS / IDlin,pMOS ratio approaches to unity as the channel length reduces. This is caused by the increase of charge density in pMOS.

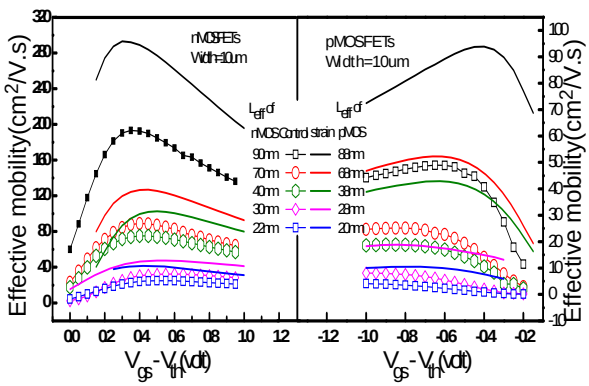


Fig. 8 The experimental results of the mobility curves for nMOS (**left**) and pMOS devices (**right**) down to 22nm. The mobility of strained devices is obviously enhanced, compared to that of the control, but all the mobility of strained devices are degraded as gate length reduces.

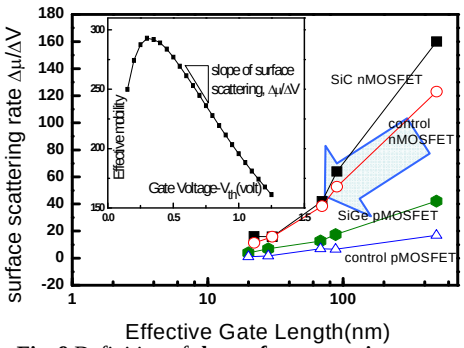


Fig. 9 Definition of **the surface scattering rate,** Δμ/ΔV.(**the insert**) The larger this parameter is; the serious the surface scatting is. The scattering rate will be smaller as the channel length reduces since the surface scattering events will be degraded when the channel length is shorter.

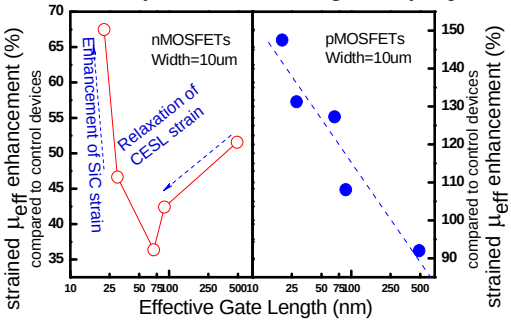


Fig. 10 (***left***)The mobility enhancement(%) of strained devices, compared to the control for nMOS, in which the mobility decay is due to the relaxation of CESL strain, and the increasing trend is owing to the enhancement of SiC strain. The (***right)*** figure shows pMOS results.

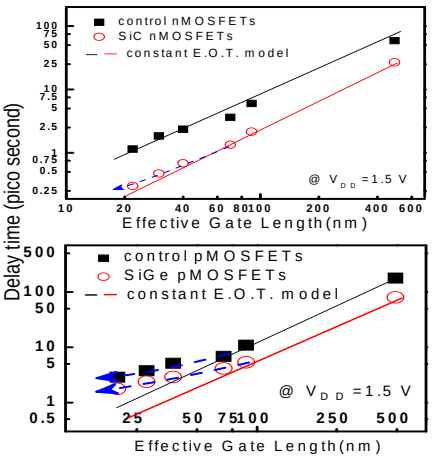


Fig. 11 The delay time of nMOS(**top**) and pMOS(**bottom**). The new results show that the delay time is flattened out, compared to the rapid decay modeled by the constant E.O.T. assumption.