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Radiation-Induced Parasitic Bipolar Effect in PMOS with Embedded SiGe

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1. Introduction

Continuous scaling of semiconductor devices has improved CMOS performance and increased the density of transistors on a chip. However, several problems have emerged with scaling down. Radiation-induced soft error is one of the crucial issues in semiconductor device reliability. In particular, radiation-induced parasitic bipolar effect has become considerable in soft error [1]. One of the reasons is that the shortening of gate length has bared a parasitic bipolar transistor that consists of source, well and drain. The schematic mechanism of this effect in PMOS is illustrated in Fig. 1. Figure 1 (a) depicts charge deposition induced by radiation and subsequent hole collection. This event causes a noise current and can lead to circuit errors. Confined electrons in n-well cause a perturbation of the n-well potential which possibly turns on the parasitic bipolar transistor and causes a large noise current (Fig. 1 (b)).

For the latest CMOS technology, embedded SiGe (eSiGe) is used in source/drain regions of PMOS as a stressor. Since the band-gap of SiGe is smaller than that of Si, the behavior of the parasitic bipolar transistors is probably different in conventional PMOS (Si PMOS) and PMOS with eSiGe source/drain (eSiGe PMOS). Therefore, it is necessary to explore the parasitic bipolar effect in them.

This work experimentally investigates soft error rates (SERs) in Si/eSiGe devices with neutron acceleration test and analyzes the characteristics of the parasitic bipolar transistors in Si/SiGe PMOS using TCAD simulation.

2. Experiments

In order to evaluate SERs on NMOS and PMOS separately, we use an unbalanced feedback-loop circuit as shown in Fig. 2. M0 and M1 are output nodes of large inverter and small inverter, respectively. Critical charge, which is minimum charge required to corrupt stored data, on M0 is extremely larger than that on M1. The contribution of M1 to total SER is dominant in this circuit. When radiation generates hole-electron pairs, NMOS in a high state collect only electrons and PMOS in a low state collect only holes. Hence, we can choose one which is more dominant on SER between NMOS (N1) and PMOS (P1) by controlling the state of the circuit ("0" or "1" state).

Test chips are manufactured in processes A, B and C. Process A includes Si PMOS. Process B and C include eSiGe PMOS. We conducted accelerated neutron tests using spallation neutron beam in Research Center for Nuclear Physics (RCNP) at Osaka University. Figure 3 shows the ratio between NMOS and PMOS SERs. This result demonstrates that the contribution of eSiGe PMOS to total SER drastically decreases comparing to that of Si PMOS. The decrease in the contribution of PMOS may be attributed to the suppression of the parasitic bipolar effect due to eSiGe source/drain.

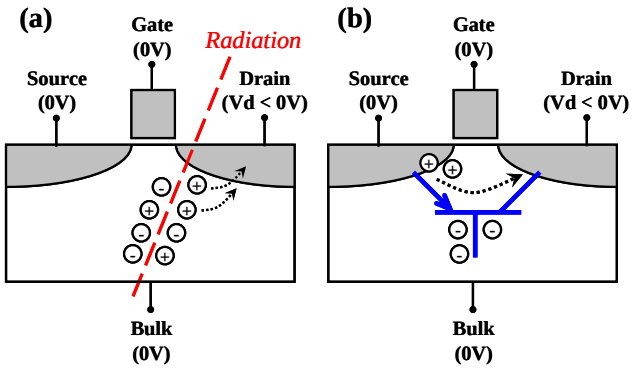

Fig. 1 Illustration of the parasitic bipolar effect in PMOS.

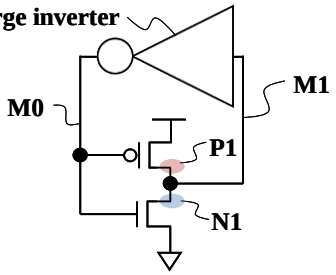

Fig. 2 Schematic of the unbalanced feedback-loop circuit.

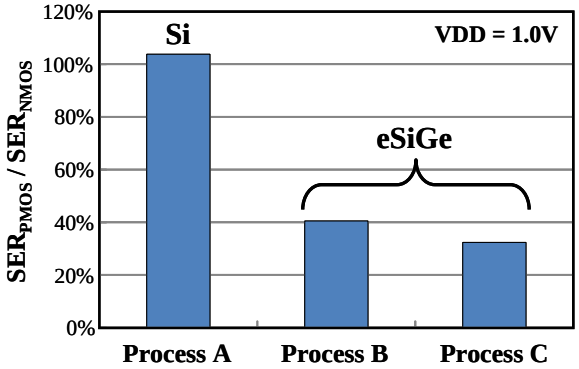

Fig. 3 The ratio between NMOS and PMOS SERs.

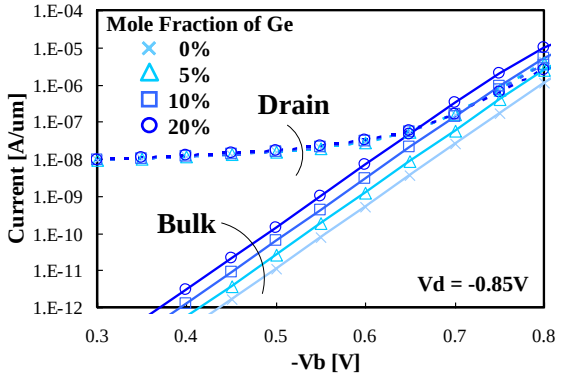

Fig. 4 Bulk bias voltage dependences of drain and bulk currents in Si/eSiGe PMOS.

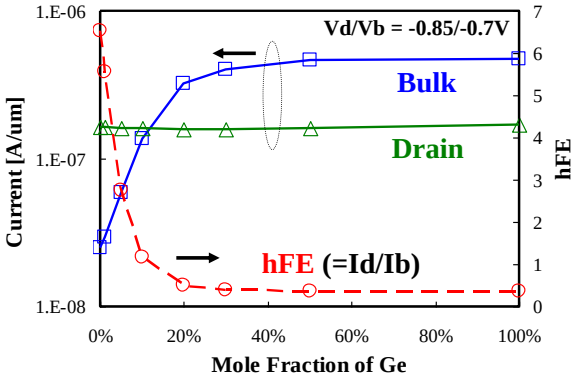

Fig. 5 Ge mole fraction dependences of drain, bulk currents and hFE in Si/eSiGe PMOS.

3. Simulations

To analyze the effect of eSiGe in PMOS on the parasitic bipolar transistor, we perform TCAD simulations using Synopsys Sentaurus package [2]. For the purpose of qualitative study, we adopt simplified PMOS structure which has eSiGe source/drain with uniform Ge mole fraction. The value of Ge mole fraction is varied from 0% to 100% while dopant profile is unaltered. In the simulations, four terminals are attached as shown in Fig. 1. Bulk bias voltage is swept to turn on the parasitic bipolar transistor. Figure 4 shows bulk bias dependences of drain and bulk currents. Figure 5 shows Ge mole fraction dependences of them. The current gain (hFE) is also shown in Fig. 5. These results demonstrate that bulk current increases with Ge mole fraction while drain current is almost unchanged. This results in the decrease of hFE with Ge mole fraction as seen in Fig. 5. In other words, the parasitic bipolar transistor loses its efficiency due to eSiGe source/drain.

4. Discussions

Figure 6 (a) and (b) show schematic band diagrams of Si and eSiGe PMOS, respectively. These diagrams correspond to the parasitic bipolar transistor depicted in Fig. 1 (b). Since the band-gap of SiGe is smaller than that of Si, a barrier height for electrons at drain (emitter) / n-well (base) interface become lower in eSiGe PMOS. The difference of the barrier height is determined by that of the band-gap

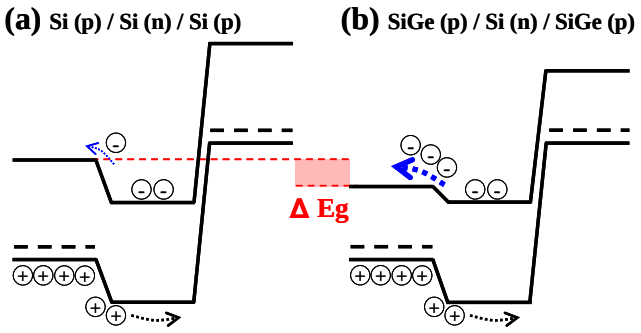

Fig. 6 Schematic band diagram of the parasitic bipolar transistor in Si/eSiGe PMOS.

(ΔEg). ΔEg increases with Ge mole fraction. We point out that this is an opposite situation of a heterojunction bipolar transistor (HBT), where wide gap semiconductors are generally used as a material of emitter. Our simulation results can be explained in analogy with a mechanism of HBT: the base current increases due to the lowering of the barrier height while the drain current remains unchanged. When considering the parasitic bipolar effect, we need to focus on the behavior of electrons in n-well. As mentioned above, the confinement of electrons generated by radiation can perturb n-well potential and possibly turn on the parasitic bipolar transistor. This means that immediate evacuation of electrons from n-well is needed for the suppression of the parasitic bipolar effect. As shown in Fig. 6, electrons in eSiGe PMOS are easier to move into source than those in Si PMOS. Due to this behavior, the perturbation of n-well potential can be prevented or can recover quickly in eSiGe PMOS. We conclude that this mechanism is probable explanation for our experimental results. In addition, we comment that it is not only for eSiGe but for any embedded materials in source/drain. For example, embedded SiC as a stressor for NMOS may affect the parasitic bipolar effect.

5. Conclusions

Accelerated neutron tests have been carried out using the unbalanced feedback-loop circuit on Si/eSiGe devices. The contribution of PMOS to total SER is shown to decrease in eSiGe devices. We have also performed TCAD simulations and found that the band-gap difference between Si and SiGe change the characteristics of the parasitic bipolar transistor. We propose that this change can lead to the suppression of the parasitic bipolar effect in eSiGe devices.

Acknowledgements

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References

[1] B. D. Olson, D. Ball, K. M. Warren, L. W. Massengill, N. F. Haddad, S. E. McMorrow, and D. Doyle, IEEE Trans. Nucl. Sci. 52 (2005) 2132.

[2] (2012) Synopsys Sentaurus TCAD tools. [Online], Available: http://www.synopsys.com/Tools/TCAD/Pages/default.aspx