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III-V 3D Transistors (invited)

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1. Introduction

III-V MOSFETs have been considered promising candidate for post-Si logic devices beyond 14nm technology node. To meet the increasing demand in electrostatic control at sub-100nm channel lengths, non-planar 3D structures have been introduced to the fabrication of III-V MOSFETs. In this paper, the fabrication and characterization of InGaAs gate-all-around nanowire MOSFETs have been demonstrated and summarized [1-2]. It is shown that the implementation of 3D structure greatly reduces short channel effect and improves scalability of InGaAs MOSFETs. The gate-all-around nanowire structure has been fabricated by a novel top-down approach for the first time and is found to offer great scalability down to at least 50nm channel length with good transport property, making InGaAs gate-all-around (GAA) nanowire MOSFETs strong candidate for ultimately scaled III-V logic technology.

2. Experiments and Results

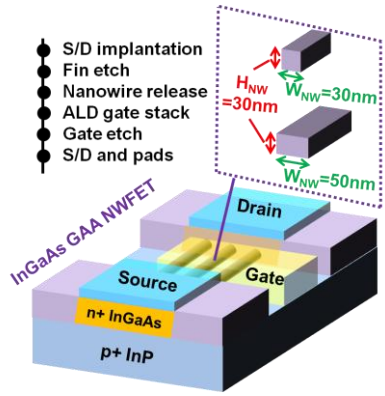

Fig. 1 Schematic diagram of InGaAs GAA nanowire MOSFETs and key fabrication process steps.

Figure 1 shows a schematic diagram as well as key fabrication processes of an InGaAs GAA nanowire MOSFET studied in this work. Fabrication started with a 30nm $In_{0.53}Ga_{0.47}As$ channel layer epitaxially grown on a heavily p-doped InP (100) substrate by molecular beam epitaxy. After source/drain implantation, fin patterning was performed using BCl_3/Ar inductively coupled plasma (ICP) etching, followed by hydrogen chloride (HCl) based nanowire release process. The nanowires were aligned along [100] direction as required by the anisotropic HCl wet etching. After surface passivation with ammonia sulfide, 10nm Al_2O_3 and 20nm WN were grown by atomic layer deposition (ALD) at temperature of 300C and 385C respectively. Due to the excellent conformal coating ability of ALD, the gate stack forms surrounding all facets of the nanowires. Gate etch using CF_4 based ICP etching was then carried out to define the gate pattern. Finally, ohmic contacts were formed by electron beam evaporation of Au/Ge/Ni and liftoff process. Two different sizes of nanowires under investigation have also been depicted in Figure 1. The larger wire has $W_{NW} \times H_{NW}$ of 50nm×30nm, and the smaller wire has $W_{NW} \times H_{NW}$ of 30nm×30nm.

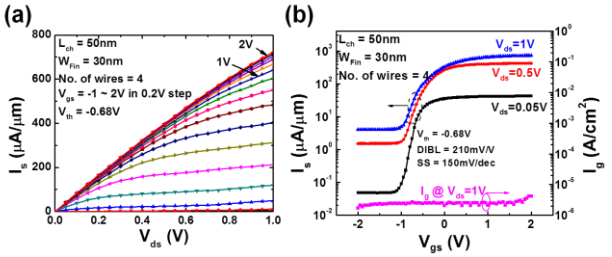

Fig. 2 (a) output and (b) transfer characteristics of InGaAs GAA FET with L_{ch}=50nm, W_{NW}=30nm.

Fig. 2 (a) and (b) show the well-behaved output and transfer characteristics as well as I_g-V_g of a L_{ch} = 50nm GAA FET. The current here is normalized by the total perimeter of the $In_{0.53}Ga_{0.47}As$ channel, i.e. $W_G = (2W_{Fin} + 2H_{Fin}) \times$ (No. of wires). A representative 50nm L_{ch} device shows on-current of 720μA/μm, transconductance of 510μS/μm and reasonable off-state characteristics with subthreshold swing (SS) of 150mV/dec and drain-induced barrier lowering (DIBL) of 210mV/V. Although operating in inversion-mode, the threshold voltage of the device is -0.68V from linear extrapolation at V_{ds}=50mV due to the relatively low work function of ALD WN metal (~4.6eV). Due to the junction leakage current and a very large area ratio (>10^3) between implanted junction and GAA channels, the source current is used to obtain the intrinsic current in the channel. Gate leakage current is minimal in the entire gate voltage range, indicating 10nm Al_2O_3 is sufficient for GAA structure and further equivalent oxide thickness (EOT) scaling is achievable. It also shows that the WN gate etch process is damage-free.

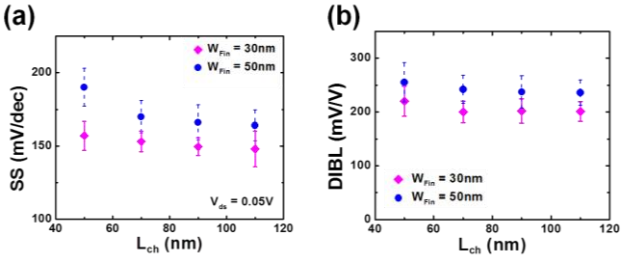

Fig. 3 (a) SS and (b) DIBL scaling metrics of InGaAs GAA FETs with L_{ch} down to 50nm.

Fig. 3 show the off-state (SS and DIBL) scaling metrics for L_{ch} = 50 - 110nm with W_{NW}=30nm and 50nm. The SS

for 30nm W_{NW} devices are almost unchanged at around 150mV/dec when scaling L_{ch} down to 50nm, indicating excellent control of SCE, whereas the 50nm W_{NW} devices show larger SS, which increases with scaling of L_{ch}. It is noted here that the 100nm L_{ch} InGaAs FinFET with 5nm Al_2O_3 gate oxide shows similar SS [3] as the 50nm L_{ch} GAA FET with 10nm Al_2O_3 in this work. This translates to at least a factor of 2 improvement of midgap Dit (~5.6×10^{12}/cm^2·eV) achieved. The improved interface quality indicates that the newly-developed channel release process can provide a smooth damage-free InGaAs bottom surface. Fig. 3(b) shows that 30nm W_{NW} devices have smaller DIBL and the DIBL is roughly independent of L_{ch}, confirming the effective SCE control. Further SS and DIBL reduction can be achieved by scaling down EOT and reducing the InGaAs nanowire dimension.

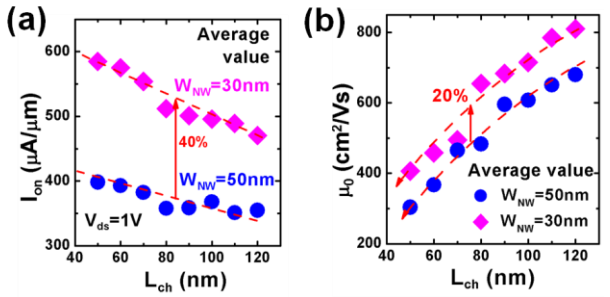

Fig. 4 (a) I_{ON} and (b) μ_0 scaling metrics of InGaAs GAA FETs with L_{ch} down to 50nm for W_{NW}=30nm and 50nm.

Figure 4(a) shows the I_{on} as a function of L_{ch} for different W_{NW}. The enhancement in on-state metrics is observed consistently regardless of the L_{ch}. An average of 40% increase in I_{on} is observed on 30nm W_{NW} devices. Furthermore, the low field mobility μ_0 is extracted using Y-function method [4]. Figure 4(b) shows the extracted μ_0 as a function of L_{ch} for W_{NW}=30nm and 50nm. 20% mobility enhancement is obtained from the smaller nanowire devices. The mobility of InGaAs GAA NWFETs is 2-3 times higher than those on Si NWFETs [5], thanks to the better transport property of III-Vs. We ascribe the enhanced on-state metrics (I_{on}, μ_0) for smaller nanowires to the volume inversion effect [2]. Due to the much smaller effective mass of InGaAs, inversion layer thickness could be 3.5 times larger than that of Si, making volume inversion easier to occur at larger nanowire dimensions.

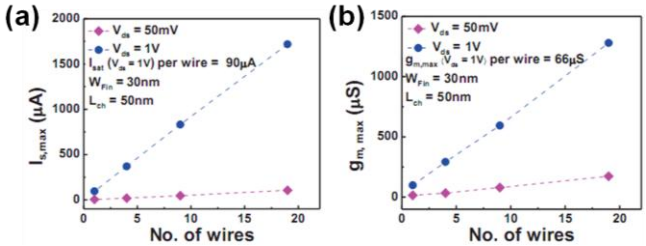

Fig. 5 (a) Linear and saturation current (b) Linear and saturation transconducatnace for GAA FETs with different number of parallel wires.

Fig. 5(a)-(b) show a linear relationship of $I_{s,max}$ and $g_{m,max}$ with the number of wires in both the linear and saturation regimes. The linear dependence demonstrates that the fabrication process is scalable towards high integration density. Each wire can deliver an I_{sat} = 90 μA and g_m = 66 μS at V_{ds}=1V.

3. Conclusion

We have demonstrated for the first time inversion-mode $In_{0.53}Ga_{0.47}As$ GAA MOSFETs with ALD Al_2O_3/WN gate stacks. Detailed scaling metrics study shows that the 3D GAA structure can effectively control the SCE with L_{ch} scaling down to at least 50nm. Nanowire size-dependent transport study reveals that volume inversion occur at larger dimension in InGaAs nanowires that its Si counterpart, making III-V GAA FET a very promising candidate for ultimately scaled III-V logic device technology.

Acknowledgment

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