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BEOL InGaAs nMOSFETs on Polyimide

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1. Introduction

Post-Si materials, such as III-V semiconductors or Ge, have been aggressively studied as promising channel materials for *n/p*MOSFETs, because of their high carrier mobilities. However, these post-Si materials cannot be replaced Si CMOS entirely. Thus, the integration technology with emerging post-Si materials on Si CMOS should be developed. From the viewpoint of the fabrication process, it is noteworthy that the maximum process temperatures of new channel materials are around 400°C that is quite lower than that of Si MOSFETs [1, 2]. Therefore, post-Si material MOFSETs can be integrated on Si CMOS wafers and get interconnected with underlying Si-based circuits in the back end of line (BEOL) process (Fig. 1).

For the feasible demonstration of the back end integration for post-Si materials, we employ the post-Si material bonding technique using polyimide (PI) polymer as an adhesive. PI is widely used the package-level integration for bonding chips because PI comprises one of the most stable and heat resistant polymer system (up to 400°C) (Fig. 2). Also, PI physically passivates and protects the semiconductor surfaces from the ambient environment while maintaining or even improving the electrical performance of the device measured prior to passivation. A number of groups have reported on the passivating behavior of PI in InGaAs/InP [3, 4, 5].

In this work, we demonstrate the low temperature fabrication of InGaAs *n*MOSFETs by using bonded InGaAs/PI/Si wafers, as the back end post-Si material integration technique. We present the operation of higher electron mobility in InGaAs *n*MOSFETs on PI with Ni-InGaAs metal S/D than those of Si MOSFETs.

2. Fabrication of InGaAs nMOSFET on Polyimide

InGaAs/PI/Si substrates were realized by utilizing the direct substrate bonding process. The schematic fabrication process is shown in Fig. 3. The epitaxial grown InGaAs /InP substrates was prepared as a donor substrate. The In content and doping concentration of the InGaAs layers were 0.53 and $3\text{x}10^{16}\text{cm}^{-3}$, respectively. InGaAs/InP wafers were pretreated using sulfur passivation with $(NH_4)_2S_x$ solutions. For a host substrate, PI with the thickness of 1.4μm was spun on the Si substrate as a bonding adhesive. Subsequently, PI/Si wafer was put on the hotplate up to at 180°C for the soft bake. After the soft bake, InGaAs/InP donor wafer was bonded onto the PI/Si substrate at 300°C for 10min with the bonding pressure of 16kgf/cm^2 in vacuum (10Pa). Finally, the InP substrate was removed by highly selective wet etching using an HCl solution. Figure 4 shows XSEM image of fabricated InGaAs/PI/Si substrate. A 300nm thick InGaAs layer was transferred on PI(1.4μm)/Si substrate, successfully.

Using InGaAs/PI/Si substrate, we have fabricated InGaAs *n*MOSFETs with Ni-based metal S/D. The schematic flow of the MOSFET fabrication process is also shown in Fig. 3. After pretreatment of the InGaAs surfaces by $(NH_4)_2S_x$ solutions, a 100-cycle Al_2O_3 layer was deposited as a gate insulator by ALD and PDA carried out at 400ºC. Next, TaN metal gate was formed by sputtering and dry etching, followed by postmetallization annealing at 350ºC. Subsequently, 25nm-thick Ni was deposited on the InGaAs layer in order to form the Ni-InGaAs metal S/D. Ni-based metal S/D for InGaAs was formed by annealing at 350ºC for 1 min, followed by selective wet etching using a HCl solution to remove the unreacted Ni. As a reference, bulk InGaAs *n*MOSFETs fabricated at the same time.

3. Electrical properties of InGaAs nMOSFET on PI

Figures 5 show the I_d–V_d and I_d–V_g characteristics of a 300nm-thick InGaAs *n*MOSFET on PI with the gate length of 50μm. The device shows good transfer and out put characteristics. We confirm that I_d values of the InGaAs *n*MOSFET on PI are almost the same as the I_s values and the S.S. is 200mV/dec. These results demonstrate the first successful operation of InGaAs nMOSFET on PI.

Figure 6 shows the electron mobilities as a function of surface charge density of the InGaAs on PI and bulk InGaAs *n*MOSFETs under the same processing. The InGaAs *n*MOSFETs even fabricated on PI show the higher electron mobility than Si MOSFET. We have demonstrated the high electron mobility of 1100 cm^2/Vs and mobility enhancements against Si of ~2.0 × for InGaAs *n*MOSFET on PI at N_s of $2.5\text{x}10^{12}$ cm^{-2}. The mobility of InGaAs on PI exhibits slightly lower than those of the bulk InGaAs at low N_s region, mainly due to the coulomb scattering at MOS interface. However, no substantial difference can be observed in the high N_s region. It means that InGaAs layer transfer with bonding technique perform without the degradation in InGaAs bulk quality. In order to realize further improvement of the channel mobility of InGaAs MOSFETs, it could be a possible solution to realize the superior MOS interfaces on PI.

4. Conclusions

In conclusion, we have demonstrated the integration and operation of InGaAs *n*MOSFETs on PI using bonding technique, Ni-based metal S/D processes, and Al_2O_3-based

TaN/Al_2O_3 metal-gate/high-*k* gate stacks. The mobility of InGaAs *n*MOSFETs are more than twice as high as those of Si MOSFETs. These results reveal that post-Si material transfer and MOSFET fabrication of BEOL offers a flexible opportunity for post-Si material integration with Si CMOS.

Acknowledgements

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References

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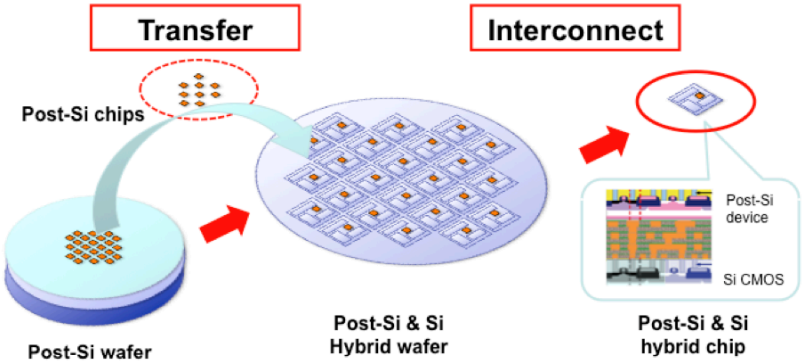

Figure 1. Post-Si material integration with Si CMOS in BEOL

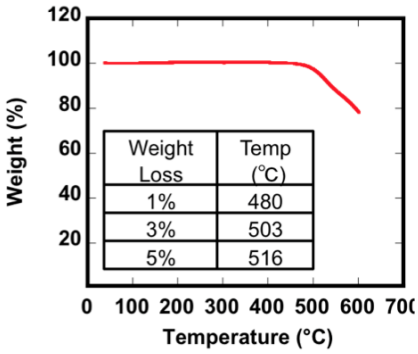

Figure 2. TGA curve in N_2 of the spin-coated polyimide film on Si.

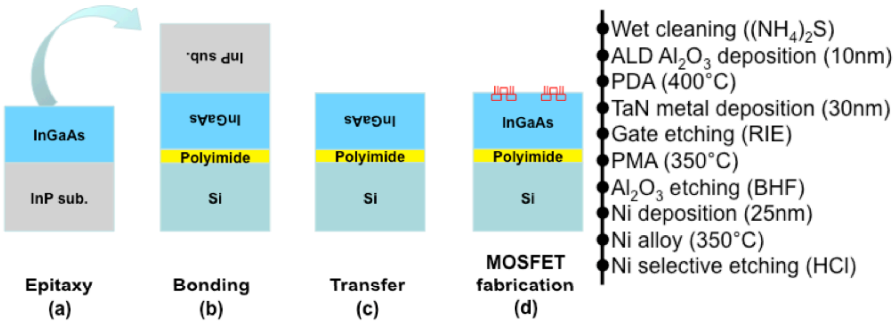

Figure 3. Process flow for fabrication InGaAs/Polyimide/Si nMOSFETs using the wafer bonding technique as a back end post-Si material integration.

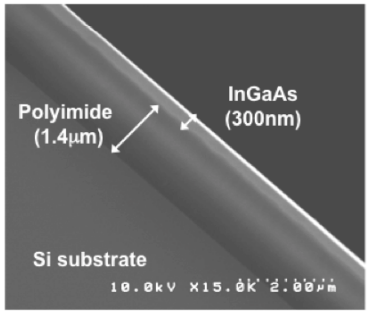

Figure 4. XSEM image of InGaAs/Polyimide/Si substrate. The thickness of InGaAs and Polyimide layers are 300nm and 1.4μm, respectively.

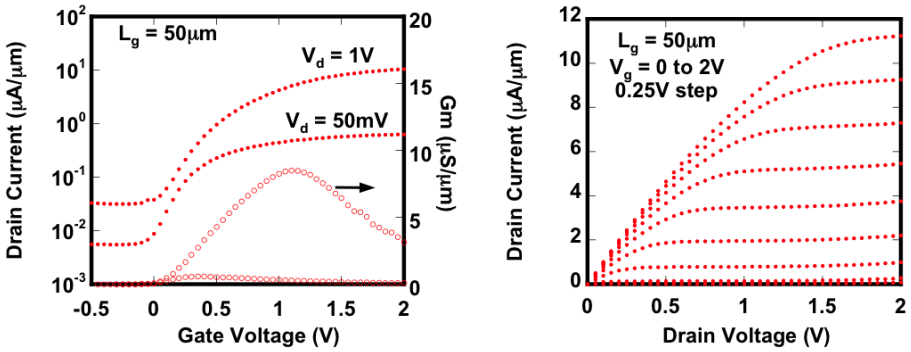

Figure 5. The I_d-V_g and I_d-V_d characteristics of InGaAs/Polyimide/Si nMOSFETs with the gate length of 50μm.

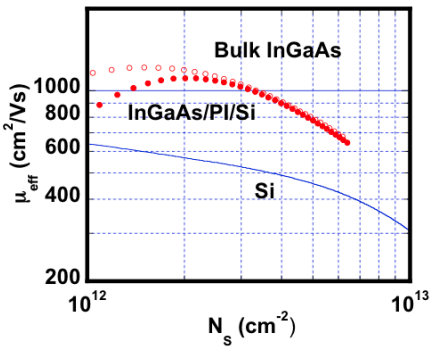

Figure 6. Mobility characteristics of InGaAs/Polyimide/Si and bulk InGaAs nMOSFETs as a function of N_S. The Si electron mobility is also shown.