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Effective Mobility Enhancement in Al_2O_3/InSb/Si Quantum Well MOSFETs for Thin InSb Channel Layers

Taihei Ito[1], Azusa Kadoda[1], Koji Nakayama[1], Yuichiro Yasui[1], Masayuki Mori[1], Koichi Maezawa[1*], Eiji Miyazaki[2] and Takashi Mizutani[2]

[1]University of Toyama, 3190 Gofuku, Toyma 930-8555, Japan
[2]Nagoya University, Furo-cho, Chikusa-ku, Nagoya 464-8603, Japan
*Phone: +81-76-445-6725 E-mail: maezawa@ieee.org

1. Introduction

InSb is attracting much attention for high-speed and low power devices in the future VLSIs, since it has highest electron mobility of 78,000 $cm^2/(Vs)$ and highest electron saturation velocity of $5x10^7$ cm/s among compound semiconductors. However, growth of high quality InSb on Si is difficult due to the large lattice mismatch of 19.3%. We have recently demonstrated that good InSb epitaxial films can be grown on Si (111) substrates using novel growth technique [1]. A key is to employ an InSb bi-layer on a Si (111) substrate as an initial layer. With this growth technique, the grown InSb layer is rotated by 30 degrees with respect to the substrate as shown in Fig. 1. This reduces the lattice mismatch to 3.3 %. This drastic reduction produces a new possibility, a pseudomorphic InSb/Si quantum well (QW) MOSFETs based on an ultra thin InSb layer grown directly on Si. We have already reported *C-V* characteristics of the MOS diodes having such thin InSb layers [2]. Furthermore, we have recently demonstrated operation of Al_2O_3/InSb/Si QW MOSFETs having a 15-nm InSb layer [3]. In this paper, we will report the dependences of the device properties, in particular the effective mobility, on the InSb channel thickness in the range from 6 to 25 nm.

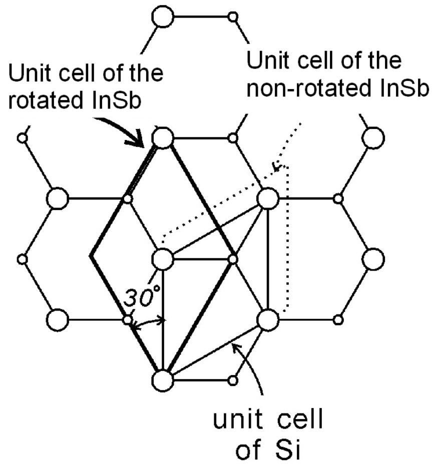

Fig. 1 Schematic view of the atom position of the Si(111) surface and the unit cells of Si and InSb

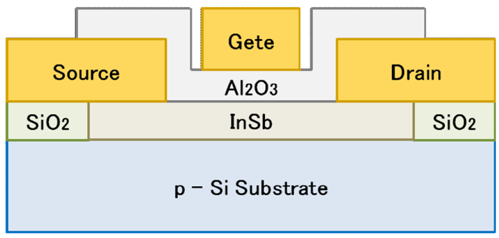

Fig. 2 Schematic cross-sectional view of the fabricated MOSFETs

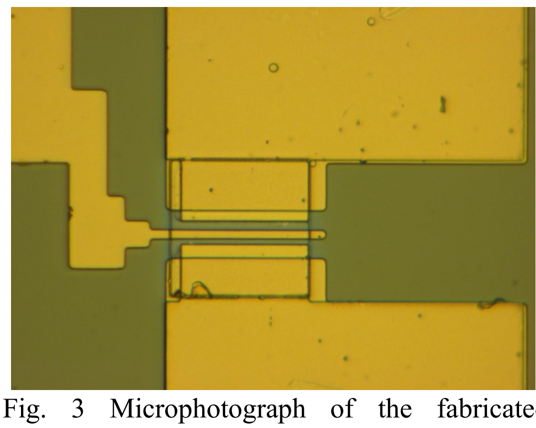

Fig. 3 Microphotograph of the fabricated MOSFETs

2. Device Fabrication

The InSb layers were grown using the surface reconstruction controlled epitaxy [1]. To prepare InSb initial bi-layer, 1 monolayer (ML) Sb was deposited onto In-induced surface reconstruction, which was formed by In deposition on to the clean Si (111) surface. The InSb films were then grown on this bi-layer. The growth temperature was initially 200 C, which is gradually increased up to 400 C . The growth rate was 0.1 nm/min, and the thicknesses were from 6 to 25 nm. The Si-substrate was p-type with a specific resistance of 10-20 Ωcm. The epitaxial layer was n-type, though no impurity was intentionally doped.

Al_2O_3/InSb/Si MOSFETs were fabricated on these epitaxial films with conventional photolithography and lift-off process. The schematic cross section of the device is shown in Fig. 2. First, the InSb layer was etched for isolation by citric acid based etchant, then the same resist pattern was used to lift off the sputtered SiO_2 layer, which insulates metal pads from the Si substrate. An Al_2O_3 gate insulator was deposited by using atomic layer deposition (ALD) at 250 C after ohmic metal formation. Thickness of the Al_2O_3 was 10 nm. Ohmic contacts were based on Sn/Au/Ni/Ti/Au metals deposited by electron beam evaporation. The devices were completed by Ti/Au gate metal formation. Figure 3 shows the microphotograph of the fabricated device.

3. Results and Discussion

An example of the FET characteristics is shown in Fig. 4. It shows the I_D-V_D characteristics of the MOSFETs having an 10-nm InSb channel. The gate length and width were 5 μm and 40 μm, respectively. A considerably large transconductance of 62 mS/mm was obtained for relatively large gate length of 5-μm. The drain current could not be suppressed when we applied the V_G of under -1 V. This is most probably due to the leakage current through the p-Si substrate.

To investigate the quality of the channel, we evaluated the effective mobility. Figure 5 shows the effective mobility as a function of the InSb channel thickness. The mobility was evaluated from the transconductance of the MOSFETs at small V_D (<0.1V). The crystal quality is expected to improve when the InSb thickness decreases in this range, because the critical layer thickness is probably around 5 nm. This result clearly demonstrates the crystal quality improvement at thinner InSb layers. The origin of the degradation at 6 nm is not yet clear, though a part of it is a large source resistance due to the thin InSb layer. Further studies are necessary.

Figure 6 shows the electron concentration of the channel when no gate bias is applied (as grown). These values were estimated from the sheet resistance measured using the TLM method and the mobility in Fig.5. As shown in the figure, the electron concentration decreases with decreasing the InSb thickness except 6-nm sample. This reduction can be explained by the reduction of the dislocation density, since the defects associated to the dislocations act as donors in InSb. It is noted that the maximum effective mobility around 1000 $cm^2/(Vs)$ for 10-nm device is rather high for the relatively large electron concentration.

4. Conclusions

The dependences of the device properties of the Al_2O_3/InSb/Si QW MOSFETs on the InSb channel thickness were investigated in the range from 6 nm to 25 nm. The enhancement of the effective mobility for thin InSb channel devices was demonstrated.

Acknowledgements

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References

[1] M. Mori et al., Jpn. J. Appl. Phys. Vol. 51, 02BH03 (2012).
[2] A. Kadoda et al., Semicond. Sci. Tech., 27 045007 (2012).
[3] K. Maezawa et al., to be presented at Device Research Conference 2012.

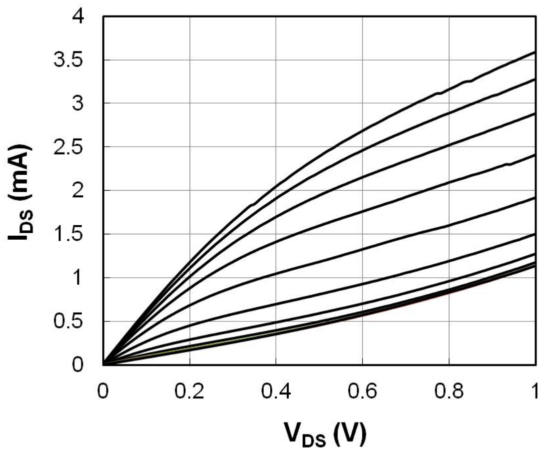

Fig. 4 I_D-V_D characteristics of the fabricated MOSFET. The gate voltage is varied from -1 V to 1V with a 0.2-V step. The gate length and width are 5 and 40 μm, respectively.

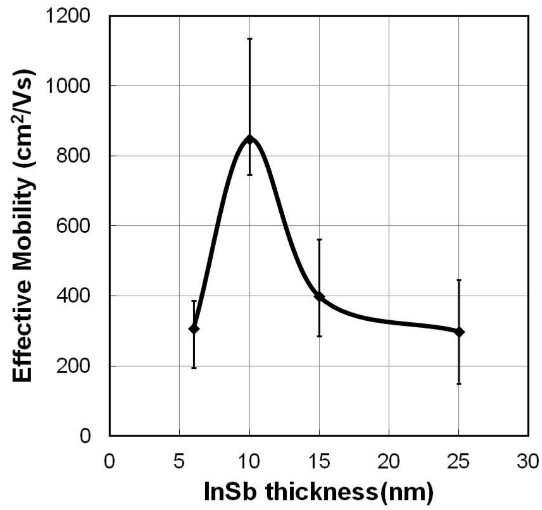

Fig. 5 Effective mobility of the fabricated MOSFETs as a function of the InSb channel layer thickness.

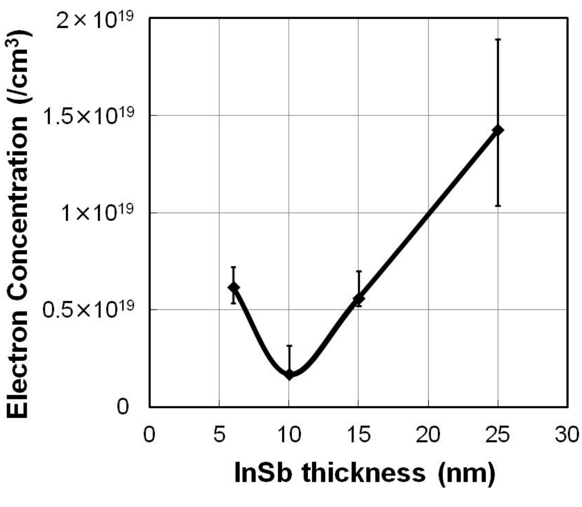

Fig. 6 Electron concentration of the InSb channel as a function of the InSb channel layer thickness.