Sub-Millimeter-Wave GaN-HEMT Technology


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1. Introduction

Recent progress of deeply-scaled GaN-HEMT technology demonstrated an unprecedented combination of high-frequency and high-breakdown characteristics, paving the way for sub-millimeter-wave power amplifier applications. This paper presents state-of-the-art high-frequency GaN-HEMT performance and key device technologies for continued scaling towards >500 GHz device operation.

2. Recent Progress of High Frequency GaN-HEMTs

For RF and mixed-signal applications, a cutoff frequency (\(f_c\)), a maximum oscillation frequency (\(f_{\text{max}}\)), maximum drain current, and a breakdown voltage (\(BV\)) are key performance parameters. Device scaling has successfully increased \(f_c\) and \(f_{\text{max}}\) of the transistors but simultaneously deteriorated \(BV\) due to associated dimension scaling. High breakdown field of GaN (\(= 3 \text{ MV/cm}\)) has been the main motivation for GaN transistors designed for power amplifiers. Figure 1 compares Johnson figure of merit (JFoM), defined as the product of \(f_c\) and \(BV\), among various high-speed device technologies. GaN-HEMTs demonstrate the highest JFoM - about 5 times higher than that of InP. The highest reported \(f_c\) for GaN-HEMTs to date is 343 GHz with a \(BV\) of 11.6 V [1].

![Fig. 1. Comparison of Johnson Figure of Merit (JFoM) among various high-speed device technologies.](image)

3. Scaling Technologies

Fig. 2 illustrates a technology cross-section of highly-scalable self-aligned-gate GaN-HEMTs. Vertically-scaled double-heterojunction (DH) HEMT epi structures consisting of Al\(_{0.35}\)Ga\(_{0.65}\)N (2.5 nm)/AIN (2.0 nm) and GaN (2.5 nm)/AIN (3.5 nm) top barriers, which are designed for E and D-mode operations, were grown on a 3-inch semi-insulating SiC substrate by MBE. Both structures have a 20-nm-thick GaN channel and an Al\(_{0.30}\)Ga\(_{0.70}\)N back barrier. The thin and high AlN top barrier layer enables to minimize the gate-to-channel distance while maintaining a high 2DEG density and a low gate leakage current. The Al\(_{0.08}\)Ga\(_{0.92}\)N back barrier was employed to increase carrier confinement, suppressing the “short-channel effect”. The E and D-mode epilayers were monolithically integrated using a selective area regrowth by MBE for mixed-signal and logic applications [2]. Highly Si-doped \(n^+\)-GaN ohmic contacts (50 nm, 7×10\(^{19}\) cm\(^{-3}\)) were regrown by MBE using a SiO\(_2\) growth mask. After removing the SiO\(_2\) mask, a Pt/Au gate self-aligned to the \(n^+\)-GaN contacts was formed using a SiN sidewall process. The gate-source and gate-drain distances defined by the thickness of the SiN sidewalls \((L_{\text{sid}})\) were fixed at 40 nm. An extremely low access resistance \((R_{\text{ac}})\) defined as a total resistance between the ohmic metal and the 2DEG of 0.1 Ω-mm was measured by TLM.

![Fig. 2. Self-aligned-gate GaN-HEMTs with \(n^+\)-GaN regrown ohmic contacts with vertically-scaled E/D-mode DH-HEMT epi structures.](image)

Fig. 3 shows output characteristics of 20-nm E and D-mode GaN-HEMTs.

![Fig. 3. Output characteristics of 20-nm E and D-mode GaN-HEMTs.](image)
20-nm E and D-mode devices, demonstrating record-high peak extrinsic $g_{m}$ of 1.63 (E) and 1.04 S/mm (D). S-parameter measurements (0.5-65 GHz) demonstrated a simultaneous $f_{T}/f_{max}$ of 343/236 GHz for the 20-nm E-mode device and 310/364 GHz for the 20-nm D-mode device (Fig. 5). Fig. 6 plots peak $f_{T}$ vs. $V_{th}$ for S-D scaled E and D-mode devices ($L_{g}/L_{ds} = 20/100$ nm) as compared to an unscaled D-mode device ($L_{g}/L_{ds} = 40/1000$ nm) [3]. The $f_{T}$ of the unscaled device peaked at around saturation voltage ($V_{sat} \approx 2$ V) and decreased monotonically with increasing $V_{th}$, while the scaled devices showed a continuous increase of $f_{T}$ with $V_{th}$ above $V_{th}$ (~0.5 V) despite their more aggressive lateral scaling. Delay time analysis attributed the improved high-frequency performance of the scaled devices and their unique dependence of $f_{T}$ on $V_{th}$ to greatly suppressed drain delay and enhanced electron velocity (Fig. 7). $f_{T}/f_{max}$ of present devices are largely limited by a high output conductance ($g_{d}$) and a large gate-drain capacitance ($C_{gd}$) associated with the lateral device dimensions. 500 GHz+ cutoff frequencies are attainable by optimizing lateral device dimensions for reduced $g_{d}$ and $C_{gd}$ in conjunction with enhanced electron supply in the source to make full use of high density-of-states of GaN material system.

4. Conclusions
Recent advances of deeply-scaled GaN-HEMT technologies were described. 20-nm self-aligned-gate GaN-HEMT technology has achieved balanced cutoff frequencies of ~350 GHz while maintaining a JFoM breakdown performance in both E and D-mode devices. GaN-HEMT technology with a continued device scaling will offer a great potential for use in sub-millimeter-wave high-power amplifier MMICs, or high-gain X-band high power amplifiers. The extremely low device access resistance will also make the technology applicable to robust low-noise amplifiers and high-speed low-loss power switch applications.

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References