F-2-1(Invited)
Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials, Kyoto, 2012, pp856-857

Sub-Millimeter-Wave GaN-HEMT Technology

K. Shinohara, D. Regan, A. Corrion, D. Brown, I. Alvarado-Rodriguez, M. Cunningham, C. Butler, A. Schmitz, S. Kim, B. Holden, and M. Micovic

HRL Laboratories, LLC
3100 Malibu Canyon Road, Malibu, CA 90265-4797, USA
Phone: +1-310-317-5093, E-mail: kshinohara@hrl.com

1. Introduction

Recent progress of deeply-scaled GaN-HEMT technology demonstrated an unprecedented combination of high-frequency and high-breakdown characteristics, paving the way for sub-millimeter-wave power amplifier applications. This paper presents state-of-the-art high-frequency GaN-HEMT performance and key device technologies for continued scaling towards >500 GHz device operation.

2. Recent Progress of High Frequency GaN-HEMTs

For RF and mixed-signal applications, a cutoff frequency (f_T), a maximum oscillation frequency (f_{max}), maximum drain current, and a breakdown voltage (*BV*) are key performance parameters. Device scaling has successfully increased f_T and f_{max} of the transistors but simultaneously deteriorated *BV* due to associated dimension scaling. High breakdown field of GaN (= 3 MV/cm) has been the main motivation for GaN transistors designed for power amplifiers. Figure 1 compares Johnson figure of merit (*JFoM*), defined as the product of f_T and *BV*, among various high-speed device technologies. GaN-HEMTs demonstrate the highest *JFoM* - about 5 times higher than that of InP. The highest reported f_T for GaN-HEMTs to date is 343 GHz with a *BV* of 11.6 V [1].

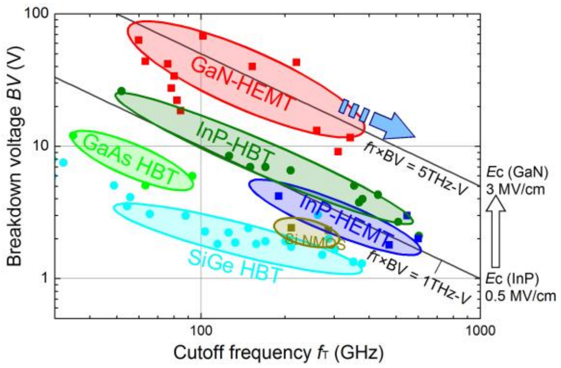

Fig. 1. Comparison of Johnson Figure of Merit (*JFoM*) among various high-speed device technologies.

3. Scaling Technologies

Fig. 2 illustrates a technology cross-section of highly-scalable self-aligned-gate GaN-HEMTs. Vertically-scaled double-heterojunction (DH) HEMT epi structures consisting of $Al_{0.5}Ga_{0.5}N$ (2.5 nm)/AlN (2.0 nm) and GaN (2.5 nm)/AlN (3.5 nm) top barriers, which are designed for E and D-mode operations, were grown on a 3-inch semi-insulating SiC substrate by MBE. Both structures have a 20-nm-thick GaN channel and an $Al_{0.08}Ga_{0.92}N$ back barrier. The thin and high AlN top barrier layer enables to minimize the gate-to-channel distance while maintaining a high 2DEG density and a low gate leakage current. The $Al_{0.08}Ga_{0.92}N$ back barrier was employed to increase carrier confinement, suppressing the "short-channel effect". The E and D-mode epitaxial layers were monolithically integrated using a selective area regrowth by MBE for mixed-signal and logic applications [2]. Highly-Si-doped n^+-GaN ohmic contacts (50 nm, 7×10^{19} cm^{-3}) were re-grown by MBE using a SiO_2 growth mask. After removing the SiO_2 mask, a Pt/Au gate self-aligned to the n^+-GaN contacts was formed using a SiN sidewall process. The gate-source and gate-drain distances defined by the thickness of the SiN sidewalls (L_{sw}) were fixed at 40 nm. An extremely low access resistance (R_{ac}) defined as a total resistance between the ohmic metal and the 2DEG of 0.1 Ω·mm was measured by TLM.

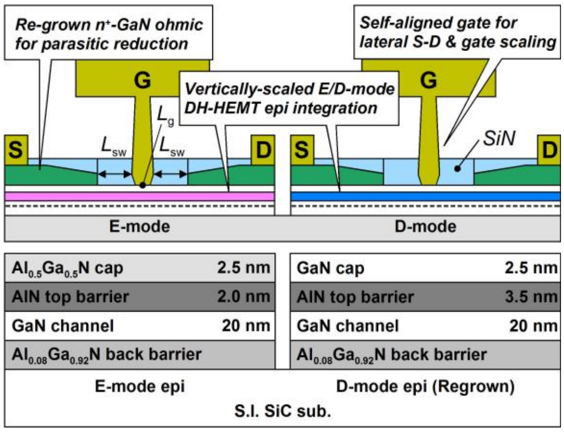

Fig. 2. Self-aligned-gate GaN-HEMTs with n^+-GaN regrown ohmic contacts with vertically-scaled E/D-mode DH-HEMT epi structures. structures.

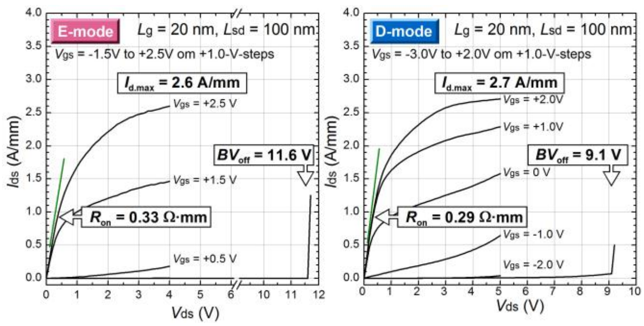

Fig. 3. Output characteristics of 20-nm E and D-mode GaN-HEMTs.

Fig. 3 shows output characteristics of 20-nm E and D-mode GaN-HEMTs, showing good pinch-off with a record-low R_{on}, high I_{dmax}, and off-state *BV* of 11.6 V (E) and 9.1 V (D). Fig. 4 shows transfer characteristics of the

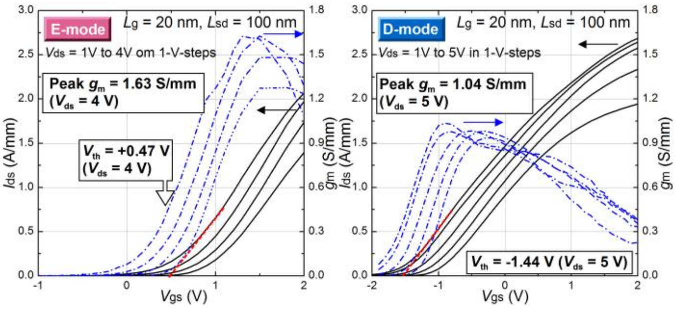

Fig. 4. Transfer characteristics of 20-nm E/D-mode GaN-HEMTs.

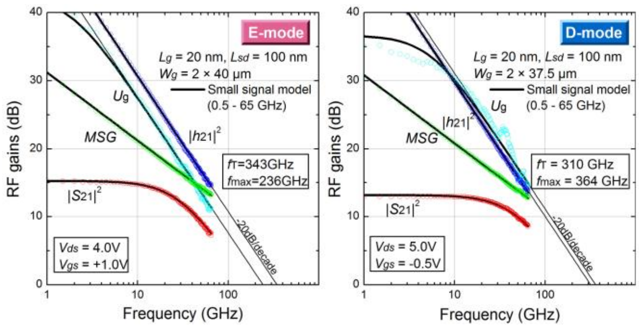

Fig. 5. Measured and modeled RF gains vs. frequency (0.5-65GHz) for 20-nm E and D-mode GaN-HEMTs.

20-nm E and D-mode devices, demonstrating record-high peak extrinsic g_m of 1.63 (E) and 1.04 S/mm (D). S-parameter measurements (0.5-65 GHz) demonstrated a simultaneous f_T/f_{max} of 343/236 GHz for the 20-nm E-mode device and 310/364 GHz for the 20-nm D-mode device (Fig. 5). Fig. 6 plots peak f_T vs. V_{ds} for S-D scaled E and D-mode devices (L_g/L_{sd} = 20/100 nm) as compared to an unscaled D-mode device (L_g/L_{sd} = 40/1000 nm) [3]. The f_T of the unscaled device peaked at around saturation voltage (V_{sat} ~2 V) and decreased monotonically with increasing V_{ds}, while the scaled devices showed a continuous increase of f_T with V_{ds} above V_{sat} (~0.5 V) despite their more aggressive lateral scaling. Delay time analysis attributed the improved high-frequency performance of the scaled devices and their unique dependence of f_T on V_{ds} to greatly suppressed drain delay and enhanced electron velocity (Fig. 7). f_T/f_{max} of present devices are largely limited by a high output conductance (g_d) and a large gate-drain capacitance (C_{gd}) associated with the lateral device dimensions. 500

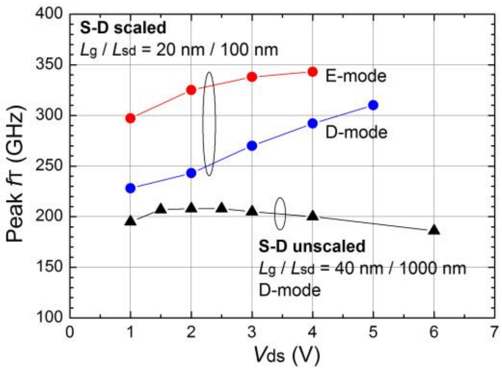

Fig. 6. Peak f_T vs. V_{ds} of S-D scaled E/D-mode devices (L_g/L_{sd} = 20/100nm) and unscaled D-mode device (L_g/L_{sd}=40/1000nm, [3]).

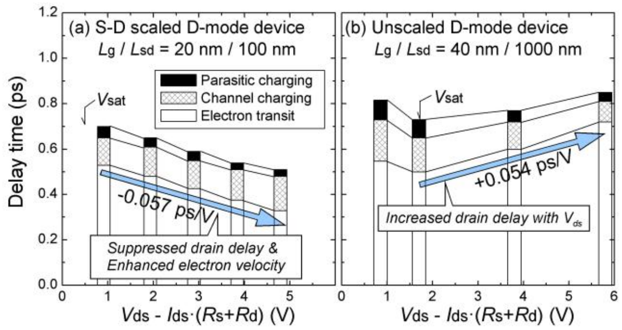

Fig. 7. Delay time components vs. channel voltage for the S-D scaled and the unscaled [3] D-mode devices.

GHz+ cutoff frequencies are attainable by optimizing lateral device dimensions for reduced g_d and C_{gd} in conjunction with enhanced electron supply in the source to make full use of high density-of-states of GaN material system.

4. Conclusions

Recent advances of deeply-scaled GaN-HEMT technologies were described. 20-nm self-aligned-gate GaN-HEMT technology has achieved balanced cutoff frequencies of ~350 GHz while maintaining a *JFoM* breakdown performance in both E and D-mode devices. GaN-HEMT technology with a continued device scaling will offer a great potential for use in sub-millimeter-wave high-power amplifier MMICs, or high-gain X-band high power amplifiers. The extremely low device access resistance will also make the technology applicable to robust low-noise amplifiers and high-speed low-loss power switch applications.

Acknowledgements

This work was sponsored by the Defense Advanced Research Projects Agency (DARPA) Nitride Electronic NeXt-Generation Technology (NEXT) program under Contract No. HR0011-09-C-0126, program manager Dr. John Albrecht. The views and conclusions contained in this document are those of the authors and should not be interpreted as representing the official policies, either expressly or implied, of the Defense Advanced Research Projects Agency or the U.S. Government.

References

[1] K. Shinohara, D. Regan, A. Corrion, D. Brown, S. Burnham, P. J. Willadsen, I. Alvarado-Rodriguez, M. Cunningham, C. Butler, A. Schmitz, S. Kim, B. Holden, D. Chang, V. Lee, A. Ohoka, P. M. Asbeck, and M. Micovic, IEDM Tech. Dig., pp.453-456 , Dec. 2011.

[2] D. F. Brown, K. Shinohara, A. Williams, I. Milosavljevic, R. Grabar, P. Hashimoto, P. J. Willadsen, A. Schmitz, A. L. Corrion, S. Kim, D. Regan, C. M. Butler, S. D. Burnham, and M. Micovic, IEEE Trans. Electron Devices, vol. 58, no. 4, pp. 1063-1067, Apr. 2011.

[3] K. Shinohara, A. Corrion, D. Regan, I. Milosavljevic, D. Brown, S. Burnham, P. Willadsen, C. Butler, A. Schmitz, D. Wheeler, A. Fung and M. Micovic, "220GHz f_T and 400GHz f_{max} in 40-nm GaN DH-HEMTs with Re-grown Ohmic," IEDM Tech. Dig., pp. 672-675, Dec. 2010.