

High Open Circuit Voltage Gain in Vertical InGaAs Channel Metal-Insulator-Semiconductor Field-Effect Transistor using Heavily Doped Drain Region and Narrow Channel Mesa

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1. Introduction

Improvement in the performance of Si-CMOS by scaling is currently close to its physical limit. To surpass this physical limit, we have proposed a vertical InGaAs channel metal-insulator-semiconductor field-effect transistor (MISFET) with an InP/InGaAs heterostructure launcher and an undoped channel [1-4].

We had previously fabricated such a device and observed a 7 MA/cm² drain current density with a 15-nm-wide channel mesa [2]. However, the open circuit voltage gain (ratio of transconductance, g_m , to output conductance, g_o) was only 0.3 because g_o was large. In this work, we report a maximum g_m/g_o of 5.7 in a device with a heavily doped drain region and narrow channel mesa.

2. Large Output Conductance

We believe that the large g_o observed in the former structure [2] was caused by the gap between the gate electrode and the drain electrode. According to the results of a Monte Carlo simulation using DAMOCLES [4], the electric field originating from a propagating electron in a channel region is mainly terminated at a gate electrode in the region sandwiched by gate electrodes. In this case, the propagating electrons do not change potential in the vertical direction in the channel region. However, the former structure had a gap between the gate electrode and the drain electrode, and the channel in this region was not sandwiched by gate electrodes. The electric field in this region was mainly by the contribution from a propagating electron terminating at the drain electrode. When the drain current increased, the potential of the channel was raised due to the space charge of the propagated electrons. Moreover, the gate length of the former structure was not very long in comparison with the width of the mesa. Band bending around the heterointerface between the source and the channel was introduced due to the space charge. Thus, electrons accumulated near the heterointerface and degraded the propagation of ballistic transportation. However, because an increase in drain voltage decreases the band bending, resulting in the decrease of accumulated electrons, a large output conductance was observed.

These problems can be solved by sandwiching the whole undoped channel region between gate electrodes and introducing a heavily doped drain region between the drain electrode and the channel region.

In addition, channel width and length influence g_o , because g_o depends on the electric field between the source and drain. If a narrow channel mesa structure could be fabricated by a selective undercut etching process, reduction of g_o is expected.

3. Structure with Heavily Doped Drain Region

To realize low g_o , we fabricated a device with a heavily doped drain region, shown in Fig. 1.

The epitaxial structure of the device consisted of an n-InP source layer with 5×10^{18} cm⁻³ carrier concentration, a 60-nm-thick i-InGaAs channel layer, and a 40-nm-thick n-InGaAs drain layer with 1×10^{19} cm⁻³ carrier concentration.

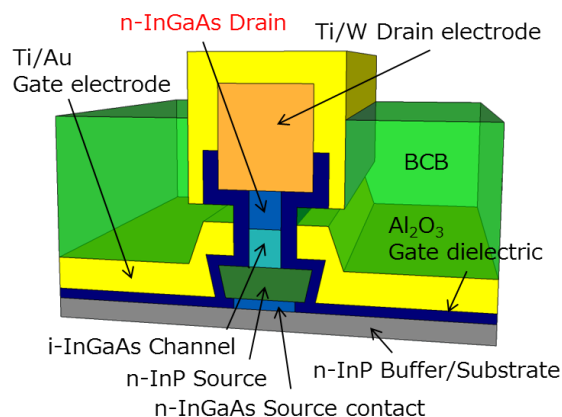


Fig. 1 Fabricated device structure.

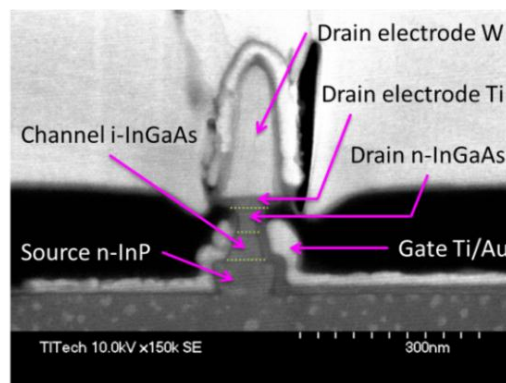


Fig. 2 SEM cross-section image of the fabricated device.

The fabrication process for the device was almost identical to that previously reported [4]. First, the Ti/W drain electrode was formed by electron beam lithography. CH₄-H₂ ICP-RIE was used for forming a narrow and vertical semiconductor mesa. Then, selective undercut etching was used to shrink the width of the channel mesa. The plasma-damaged regions were removed simultaneously. A 7.5-nm-thick Al₂O₃ layer was used as the gate dielectric, and the equivalent oxide thickness was approximately 4 nm. To fabricate the gate electrode, Ti/Au was deposited by angled evaporation in self-alignment mode. The fabricated mesa was covered by a BCB layer and the top of the drain electrode was exposed by an etch-back process. After formation of contact holes for the source electrodes and gate electrodes, contact pads and wiring were created.

The SEM cross-section image of the fabricated device is shown in Fig. 2. The presence of an undoped channel region sandwiched by Ti/Au gate electrodes was confirmed. A device with a heavily doped drain region was fabricated previously [4], but g_m/g_o was limited to 4.0 because of the relatively wide mesa (width: 45 nm). In this work, the fabricated vertical MISFET had a 23-nm-wide channel mesa as shown in Fig. 2.

Figure 3 shows the I-V characteristics of the fabricated device, measured at room temperature. A clear drain current modulation by the gate voltage was observed. The observed maximum drain current density J_d was 0.74 MA/cm² (0.17 A/mm) at $V_{ds} = 0.75$ V and $V_{gs} = 1.0$ V. Figure 4 shows g_m , g_o , and g_m/g_o of the fabricated device at $V_{ds} = 0.6$ V. The observed g_o was smaller than 0.06 S/mm when the current density was less than 0.3 MA/cm² (0.07 A/mm), while the g_o of former devices was over 0.5 S/mm at the same current level. The maximum g_m/g_o was 5.7 at $J_d = 0.146$ MA/cm² ($V_{ds} = 0.6$ V and $V_{gs} = 0.28$ V).

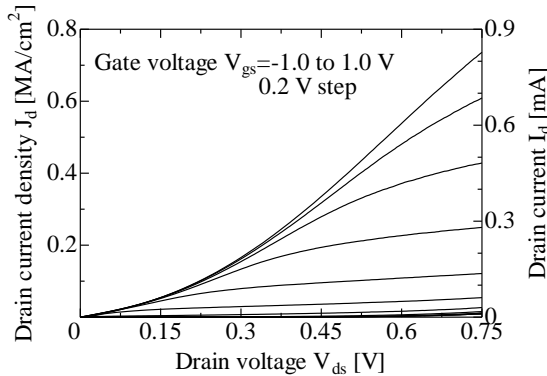


Fig. 3 I-V characteristics of the fabricated device.

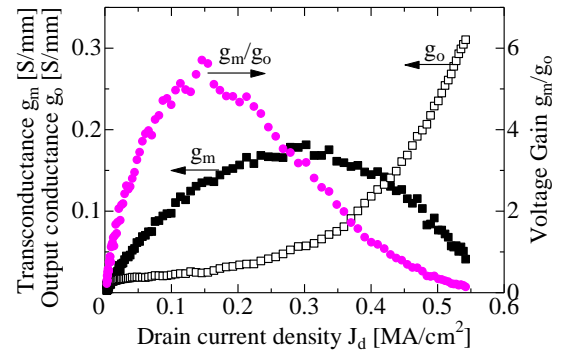


Fig. 4 Observed g_m , g_o , and g_m/g_o of the fabricated device at a V_{ds} of 0.6 V.

Table 1 shows a comparison between the observed characteristics of the fabricated device with those of the reported device with $J_d = 7$ MA/cm² [2]. In this work, g_m/g_o and the subthreshold slope (SS) were improved, although the values of J_d and g_m were reduced. As shown in Fig. 2, the side facet of the InGaAs channel region was not vertical and the width of the mesa became larger at the bottom. This wide bottom may have degraded the J_d and g_m .

4. Conclusions

In our former study, the vertical MISFET with a 15-nm-wide channel mesa showed an open circuit voltage gain of only 0.3 because of the large output conductance. In this work, we fabricated a device with both a heavily doped drain region and a 23-nm-wide channel mesa. Reduction of the output conductance was observed, and the open circuit voltage gain increased to 5.7.

Acknowledgements

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References

- [1] Y. Miyamoto et al., Jpn. J. Appl. Phys. **42** (2003) 7221.
- [2] H. Saito et al., Appl. Phys. Express **3** (2010) 084101.
- [3] H. Saito et al., Jpn. J. Appl. Phys. **50** (2011) 014102.
- [4] H. Saito and Y. Miyamoto, Appl. Phys. Express **5** (2012) 024101.

Table 1 Comparison between the observed characteristics with those of the former device.

	J_d	g_m	SS	g_m/g_o
This work	0.74 MA/cm ²	227 mS/mm	134 mV/dec	5.7
The device with 7 MA/cm ² [2]	7 MA/cm ²	550 mS/mm	650 mV/dec	0.3