Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials, Kyoto, 2012, pp872-873

120-GHz-band InP HEMT Amplifier with Gain-Enhanced Topology

Masaru Sato, Shoichi Shiba, Hiroshi Matsumura, Yasuhiro Nakasha,
Toshihide Suzuki, and Naoki Hara

Fujitsu Ltd.
10-1, Morinosato-Wakamiya, Atsugi, Kanagawa, Japan
Phone: +81-46-250-8244 E-mail: sato.masaru@jp.fujitsu.com

1. Introduction

Recently, developments of sub-millimeter-wave applications such as a 120-GHz-band 10-Gbit/s wireless link [1] and an F-band passive imaging sensor [2] are actively being developed. Low noise amplifiers (LNAs) are the key components for these systems, because they are placed at the RF front-end of every receiver. High gain with a low-noise-figure (NF) is required for LNAs. In addition, a small variation in a group delay for a wide bandwidth is also required for high-data-rate transmission. The reported wideband LNAs employ a feed forward noise cancellation technique [3-4]. Single-ended to differential conversion was performed by placing a common-gate stage in parallel to a common-source stage [3] or a CMOS inverter [4]. Although signals are amplified by the following differential amplifiers, parts of noise derived from the first stage transistor can be cancelled. However, these topologies suffer from amplitude and phase imbalance in the first stage, which will deteriorate distortion and the NF of the amplifiers.

In this paper, we proposed a new amplifier topology. A transformer-based balun was utilized at the input port. One of the outputs of the transformer is connected to the transistor's source terminal. The other output of the transformer is connected to the gate terminal via a DC block capacitor. Using this configuration, an enhanced-gain characteristic over a wide frequency range is realized.

2. Amplifier Design

Fig. 1 shows the simplified schematic of the proposed amplifier (biasing not shown). It consists of a transformer-based balun and a transistor. A single-ended input signal is applied to the transformer's input, and the outputs of the balun are led to the gate and source terminals of the transistor. Here, a DC block capacitor was inserted between the balun's output and the gate terminal. The diameter and the line width of the transformer were carefully chosen in order to operating as the balun around 120-GHz. As the balun was a passive device, low amplitude and phase imbalance can be realized using EM-simulation. The transformer also works as a current sink. The drain current flows to the ground at the center tap of the transformer.

The amplifier works as both a common-gate amplifier and common-source amplifier. Fig. 2 shows the equivalent circuit of the proposed amplifier. When viewed from the source terminal, it can be seen that the amplifier works as common-gate amplifier. Conversely, when viewed from the gate terminal, it can be seen that the amplifier works as a common-source amplifier. As differential signals are input to the source and gate terminals (because balun outputs are connected), each signal can be combined and amplified at the drain terminal.

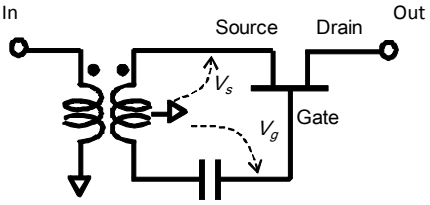

Fig. 1 Schematic diagram of the proposed LNA.

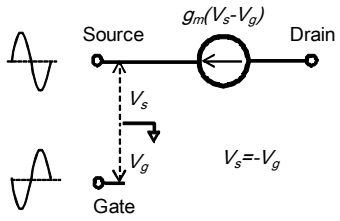

Fig. 2 Equivalent circuit of the amplifier.

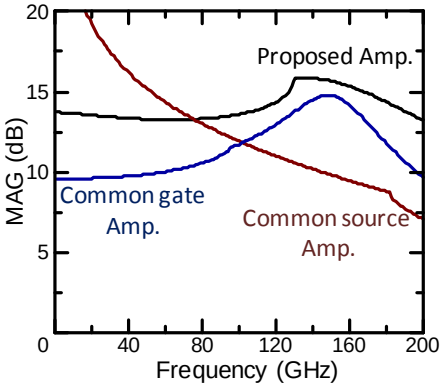

Fig. 3 Maximum available gain (MAG) characteristics of different amplifier topologies.

Fig. 3 shows the maximum available gain (MAG) of the proposed amplifier. The MAGs of the conventional common-source and common-gate amplifiers are also shown for comparison. For these simulations, the same transistors were used. The proposed amplifier exhibits higher gain

over 100 GHz than conventional amplifiers. In order to validate this design methodology, we designed and fabricated a 2-stage amplifier. Fig. 4 shows the schematic diagram of the 2-stage amplifier.

3. Device fabrication

A 75-nm InP HEMT technology [5] was used for designing 120-GHz-band amplifier. The current cutoff frequency (f_T) of a 75-nm InP HEMT was 390 GHz. For the amplifier design, we used the EE-HEMT model for the transistor model.

The conductor layer for two-layer routing was made of Au. The interlayer insulator was BCB, having a relative permittivity of 2.8.

Fig. 5 shows a chip photograph of the 120-GHz-band amplifier MMIC. The chip size was 0.63 × 0.5 mm. The core circuit size was 0.35 × 0.16 mm.

4. Measurement results

The on-wafer measurement was performed using VNAs. Below 110 GHz, 8510XF was used. From 110 to 170 GHz, PNA with VDI frequency extenders was used. Fig. 5 shows the measured S-parameters of the amplifier. The maximum gain of 12 dB was obtained at 100 GHz. A -3 dB bandwidth of over 40 GHz was obtained from 93 to over 133 GHz. S_{11} and S_{22} remain less than -10 and -7 dB, respectively. The applied bias voltage was 1.0 V, and the power consumption was 22 mW.

5. Conclusions

In this paper, an InP HEMT amplifier with enhanced gain topology was described. A transformer-based balun was utilized at the input stage. And the converted differential signals were led to transistor's gate and source terminal, and they were amplified. This topology realized a higher gain compared with a conventional common-gate or common-source amplifier. Fabricated in the 75-nm InP HEMT technology, the amplifier exhibits a gain of 12 dB and a bandwidth from 93 to 133 GHz.

Acknowledgements

The authors would like to thank Ei Yano for supports. The authors would like to thank the device processing group, Fujitsu Laboratories Ltd. This work was partially supported by the Ministry of Internal Affairs and Communications, Japan.

References

[1] H. Takahashi, T. Kosugi, A. Hirata, K. Murata, and N. Kukutsu, *Proceedings of the 3rd European Microwave Integrated Circuits Conference* (2008) 430.

[2] S. Koch, M. Guthoerl, I. Kallfass, A. Leuther, and S. Saito, *IEEE Journal of Solid-State Circuits*, Vol. 45, No. 10, (2010) 1961.

[3] H. Wang, L. Zhang, and Z. Yu, *IEEE Transactions on Circuits and Systems*, Vol. 57, No. 8, (2010) 1993.

[4] S. Saeedi, and M. Atarodi, *IEICE Trans. Electron*, Vol. E95-C, No. 1, (2012) 146.

[5] T. Takahashi, M. Sato, Y. Nakasha, T. Hirose, and N. Hara, *IEEE Elec. Device Let.*, vol. 33, no. 2, (2012) 206.

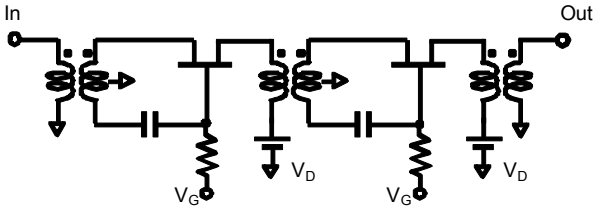

Fig. 4 Schematic of the two-stage gain-enhanced amplifier

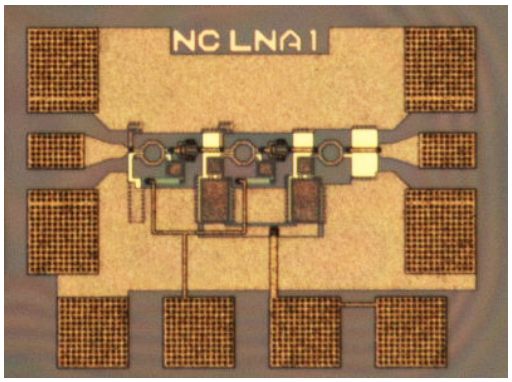

Fig. 4 Chip photograph of the fabricated amplifier. The chip size was 0.63 × 0.5 mm.

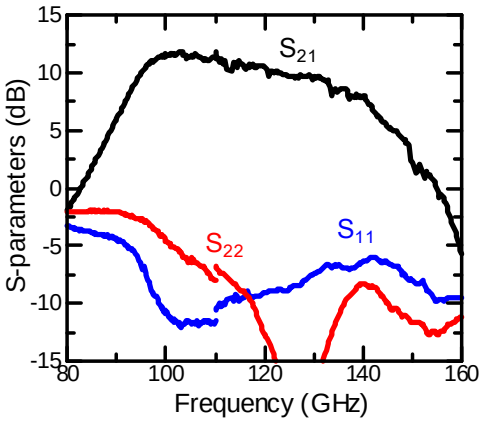

Fig. 5 Measured S-parameters of the 120-GHz-band amplifier.