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AlGaN/GaN-on-Sapphire MOS-HEMTs with Breakdown Voltage of 1400 V and On-State Resistance of 22 mΩ.cm^2 using a CMOS-Compatible Gold-Free Process

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1. Introduction

AlGaN/GaN Metal-Oxide-Semiconductor High-Electron Mobility Transistors (MOS-HEMTs) are attractive for high power electronic applications. However, most of the AlGaN/GaN devices reported in the literature were fabricated using a non-gold-free process, where gold was used either as gate or source/drain contacts [1]-[9]. In order to fabricate GaN devices in Si fabs without gold contamination, CMOS-compatible gold-free processes for fabricating AlGaN/GaN devices are needed. In addition, different approaches were proposed to reduce the gate leakage current I_G, such as inserting a gate dielectric under the gate (I_G ~ 5×10^{-10} A/mm) [10] and O_2 plasma treatment (I_G ~ 6×10^{-9} A/mm) [11].

In this paper, we report the realization of AlGaN/GaN-on-sapphire MOS-HEMTs with off-state breakdown voltage V_{BR} of 1400 V and on-state resistance R_{on} of 22 mΩ.cm^2 using a CMOS-compatible gold-free process. In addition, devices achieved high on/off current ratio I_{on}/I_{off} of 10^9 and low I_G of 10^{-11} A/mm. Compared to those of gold-free AlGaN/GaN MOS-HEMTs reported in literature, the V_{BR} achieved in this work is the highest.

2. Device Fabrication: CMOS-Compatible Gold-Free Process

Fig. 1 shows a gold-free process flow for fabricating the AlGaN/GaN-on-sapphire MOS-HEMTs with a TaN metal gate. 2-inch undoped $Al_{0.25}Ga_{0.75}N$(25 nm)/i-GaN(2.7 μm)/Fe-doped GaN (300 nm) epitaxial layers on sapphire substrate was used. After mesa etching using Cl_2-based reactive ion etching, 10 min native oxide removal using dilute HCl (HCl:H_2O = 1:1) and 30 min *ex situ* surface passivation treatment using $(NH_4)_2S$ solution were performed.

An Al_2O_3 gate dielectric (15 nm) was deposited by Atomic Layer Deposition. Post Deposition Anneal (PDA) at 450 ºC for 60 s in N_2 ambient was then performed, followed by reactive sputter deposition of TaN metal and gate patterning using Cl_2-based dry etching. The gate stack formation is CMOS-compatible. A Pt(100 nm)/Ti(10 nm)/Al(120 nm)/Ti(20 nm) metal stack was deposited and patterned in the source/drain contact regions. An alloying process at 650 ºC for 30 s in N_2 ambient was used to form ohmic contacts.

3. Results and Discussion

Fig. 2 shows the schematic view of an AlGaN/GaN-on-sapphire MOS-HEMT. Gate-to-drain spacing and gate-to-source spacing are defined as L_{GD} and L_{GS}, respectively. Fig. 3 (a) and (b) show linear *I-V* characteristics of the fabricated transmission line method (TLM) test structure, sheet resistance R_{sh} of 527 Ω/square and specific contact resistivity ρ_c of 4.5 × 10^{-3} Ω.cm^2 was obtained.

Fig. 4 shows the gate leakage current density J_G as a function of gate voltage V_G. J_G is capped at ~10^{-5} A/cm^2 for V_G from 0 to -20 V. Fig. 5 shows the transfer (I_D-V_G) and transconductance (g_m-V_G) characteristics of an AlGaN/GaN MOS-HEMT (L_G = 2 μm, and L_{GS} = L_{GD} = 5 μm). Sub-threshold swing *S*, peak g_m at V_D = 5 V, and threshold voltage V_{th} are 89 mV/decade, 20.4 mS/mm and -2.6 V, respectively. Fig. 6 shows output (I_D-V_D) characteristics of the same AlGaN/GaN MOS-HEMT shown in Fig. 5, where V_G is varied in steps of 1 V from -2 V to 2 V.

Fig. 7 shows sub-threshold swing *S* (left axis) and I_{on}/I_{off} ratio (right axis) as a function of gate leakage current I_G for AlGaN/GaN MOS-HEMTs (L_G = 2 μm, and L_{GS} = L_{GD} = 5 μm). I_{on} and I_{off} are defined to be the values of I_D measured at V_G = (V_{th} + 4) V and (V_{th} - 7) V, respectively, at V_D = 5 V. I_G is the gate leakage current at V_G = (V_{th} - 7) V and V_D = 5 V. I_{on}/I_{off} and I_G is in the range of 1.67×10^8 ~ 2.89×10^9 and 3.77 × 10^{-11} ~ 1.15×10^{-10} A/mm, respectively. Fig. 8 and 9 show the dependence of on-state resistance R_{on}, on-state drain current $I_{D,on}$ at V_D = 1 V, and off-state current $I_{D,off}$ at V_D = 1 V on the gate-to-drain spacing L_{GD}, where the gate length L_G of 2 μm and the gate-to-source spacing L_{GS} of 5 μm are fixed. As L_{GD} increases from 5 μm to 20 μm, average R_{on} is increased from 10 to 22 mΩ.cm^2; $I_{D,on}$ is reduced by 5%; $I_{D,off}$ is reduced from 6.2×10^{-10} to 4.5×10^{-11} A/mm.

Fig. 10 shows the results of a three terminal off-state high voltage measurement in Fluorinert ambient. Below V_D = 900 V, the value of I_D and I_S are almost equal, and the value of I_G is around 1 to 2 orders of magnitude lower than those of I_D and I_S. Above V_D = 900 V, I_G starts to increase and eventually reaches almost the same value as I_D, while I_S still remains constant. Above V_D = 900 V, I_D is dominated by I_G, which indicates that the breakdown occurs in the gate region. Mechanism of breakdown could be due to an avalanche breakdown or impact ionization at the drain side of the gate edge [12]. I_D remains ~ 8 × 10^{-6} A/mm when V_D is increased up to 1400 V. Breakdown voltage V_{BR} is defined as the value of V_D at which I_D reaches 1 mA/mm with the gate biased below V_{th}. Fig. 11 and 12 show a comparison of V_{BR} versus R_{on}, and V_{BR} versus L_{GD} between this work and other state-of-the-art AlGaN/GaN MOS-HEMTs [13]-[15].

4. Summary

AlGaN/GaN-on-sapphire MOS-HEMTs with V_{BR} of 1400 V and R_{on} of 22 mΩ.cm^2 were realized using a CMOS-compatible gold-free process. Process modules commonly used in CMOS fabrication were used, including TaN gate stack formation, etching modules, etc. Compared to those of gold-free AlGaN/GaN MOS-HEMTs, the V_{BR} achieved here is the highest.

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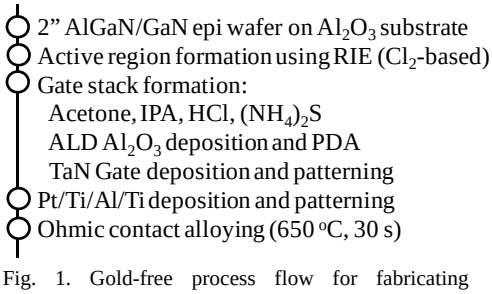

Fig. 1. Gold-free process flow for fabricating AlGaN/GaN-on-sapphire MOS-HEMTs with a TaN metal gate.

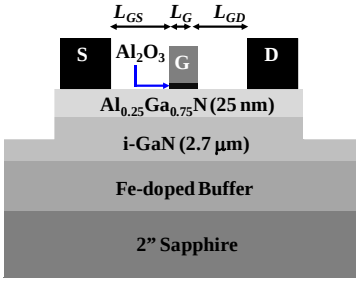

Fig. 2. Schematic view of an AlGaN/GaN-on-sapphire MOS-HEMT.

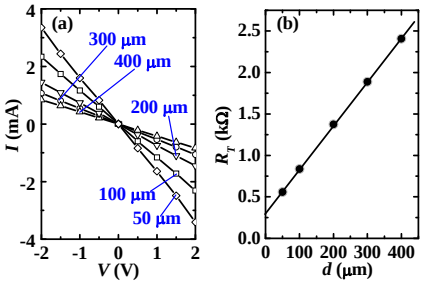

Fig.3. (a) Current-voltage (I-V) characteristics at various contact spacing d. (b) Contact resistance R_T as a function of various contact spacing d on the TLM structure after annealing at 650 °C for 30 s.

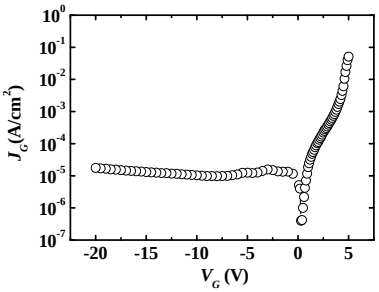

Fig. 4. Gate leakage current density J_G as a function of gate voltage V_G, when source and drain are grounded. In the negative gate voltage regime, J_G is capped at ~10^{-5} A/cm^2.

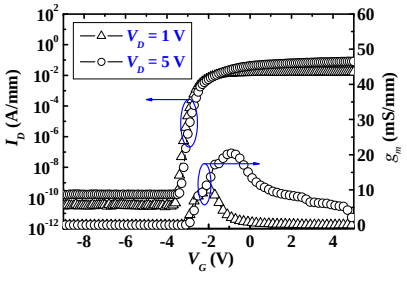

Fig. 5. Transfer (I_D-V_G) and transconductance (g_m-V_G) characteristics of AlGaN/GaN MOS-HEMT (L_G = 2 μm and L_{GS} = L_{GD} = 5 μm). Sub-threshold swing S is 89 mV/decade, peak g_m is 20.4 mS/mm at V_D = 5 V, and threshold voltage V_{th} is -2.6 V.

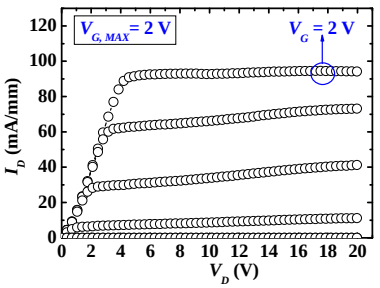

Fig. 6. Output (I_D-V_D) characteristics of the same AlGaN/GaN MOS-HEMT used in Fig. 5, where V_G is varied in steps of 1 V from -2 V to 2 V.

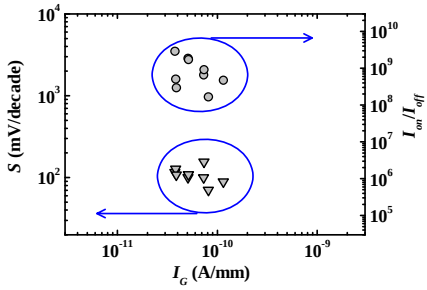

Fig. 7. Subthreshold swing S (left axis) and I_{on}/I_{off} ratio (right axis) as a function of gate leakage current I_G for AlGaN/GaN MOS-HEMTs (L_G = 2 μm and L_{GS} = L_{GD} = 5 μm).

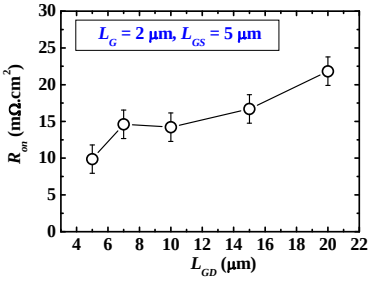

Fig. 8. On-state resistance R_{on} of AlGaN/GaN MOS-HEMTs (L_G = 2 μm and L_{GS} = 5 μm) as a function of gate-to-drain spacing L_{GD}.

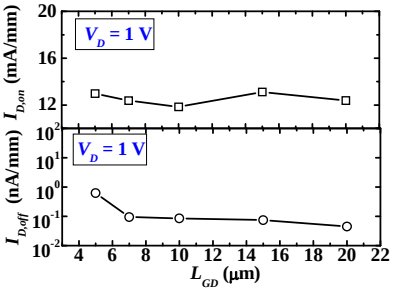

Fig. 9. $I_{D,on}$ and $I_{D,off}$ of AlGaN/GaN MOS-HEMTs (L_G = 2 μm and L_{GS} = 5 μm) as a function of gate-to-drain spacing L_{GD}. $I_{D,on}$ and $I_{D,off}$ are defined to be the values of I_D measured at V_G = 1 V and -10 V, respectively, at V_D = 1 V.

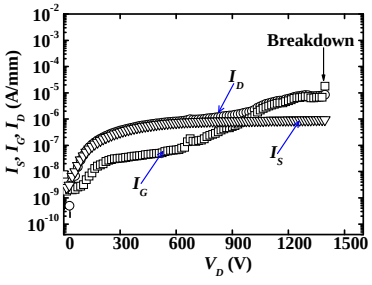

Fig. 10. I_S, I_G, and I_D as a function of V_D for three terminal off-state measurement in Fluorinert ambient (L_G = 2 μm, L_{GS} = 5 μm, and L_{GD} = 20 μm), where V_S = 0 V and V_G = -10 V. The drain current I_D is below 1 mA/mm when V_D = 1400 V.

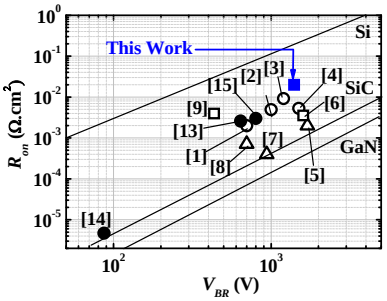

Fig. 11. Breakdown voltage V_{BR} versus on-resistance R_{on} of fabricated AlGaN/GaN MOS-HEMTs, as compared to those of state-of-the-art AlGaN/GaN MOS-HEMTs. (Open symbol: GaN MOS-HEMTs with gold; Solid symbol: GaN MOS-HEMTs without gold. Square: GaN-on-sapphire; Triangle: GaN-on-SiC; Circle: GaN-on-silicon)

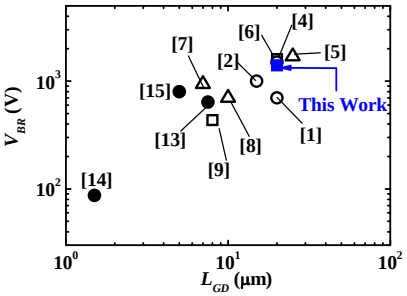

Fig. 12. Breakdown voltage V_{BR} versus gate-to-drain spacing L_{GD} of fabricated AlGaN/GaN MOS-HEMTs, as compared to those of state-of-the-art AlGaN/GaN MOS-HEMTs. (Open symbol: GaN MOS-HEMTs with gold; Solid symbol: GaN MOS-HEMTs without gold. Square: GaN-on-sapphire; Triangle: GaN-on-SiC; Circle: GaN-on-silicon)