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Improvement of current collapse by surface treatment and passivation layer in p-GaN gate GaN HEMT

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1. Introduction

Gallium Nitride (GaN) is an excellent candidate for electronic power devices due to its superior properties, such as high breakdown voltage, high electron peak saturation velocity, and high electron density compared to silicon (Si) [1-2]. In particular, AlGaN/GaN high electron mobility transistor (HEMT) power devices are suitable for use in a power conversion in hybrid and electric vehicles (HV/EV), and over 3V normally off operation devices are required in the electronic devices of vehicles [3].

Schottkty-gate GaN HEMT and insulated-gate with recess GaN HEMT have been studied to obtain the normally-off operation [1-3], but still have some problems. Schottkty-gate GaN HEMT is a simple structure, therefore, the existence of 2DEG under the gate electrode prevents the normally-off operation. On the other hand, insulated-gate with recess GaN HEMT has low 2DEG under the gate electrode, but it is difficult to control the recess depth. Recently, a p-GaN gate GaN HEMT is also proposed for the normally-off operation [4-5]. In this structure, 2DEG is easy to be depleted under gate electrode, therefore the device can operate in normally-off mode. However, the increase of current collapse is suspected in p-GaN gate GaN HEMT, because the part of p-GaN layer must be etched to form the island p-GaN gate structure. As a consequence, it is suspected that the damage causes the increase of current collapse.

In order to study the relation between the current collapse and the surface damage of p-GaN gate GaN HEMT, the current collapse of the devices with/without NH_3 treatment and high temperature oxide (HTO) passivation layer are measured.

2. Experiments

Device structure

p-GaN gate GaN HEMTs were fabricated on an p-GaN/AlGaN/GaN heterostructure grown by MOCVD on an a-plane sapphire substrate. The schematic cross sections of the devices are shown in Fig. 1. The Al content in AlGaN was 0.18. Mg doping concentration of p-GaN layer is $2x10^{19}$ cm^{-3}. A part of p-GaN layer was etched by inductively coupled plasma (ICP). The device of Fig.1(a) has no NH_3 treatment and no HTO passivation layer on AlGaN layer. The device of Fig.1(b) has NH_3 treatment on AlGaN layer. The device of Fig.1(c) has NH_3 treatment and HTO passivation layer. The expected effects of NH_3 treatment and HTO passivation layer were incorporation of nitrogen into nitrogen vacancies in AlGaN layer damaged by ICP and low interface states, respectively. Ti/Al layers used as source and drain electrodes were deposited and annealed at 650 ^oC for 5 min in N_2 ambient to ensure the formation of an ohmic contacts. The device structure is concentric circle. The gate-source length L_{GS}, gate length L_G, gate-drain length L_{GD} and gate width W_G were 2, 10, 10 and 360 μm, respectively. V_g-I_d characteristic of device (c) in Fig.1 under the drain voltage of 1V is shown in Fig. 2. The threshold voltage V_{th} of the device was 0.4V. The other two devices have also the same of V_{th}. Fig. 3 shows V_d-I_d characteristic of device(c) in Fig.1. The on resistance R_{on} is 14 $m\Omega cm^2$.

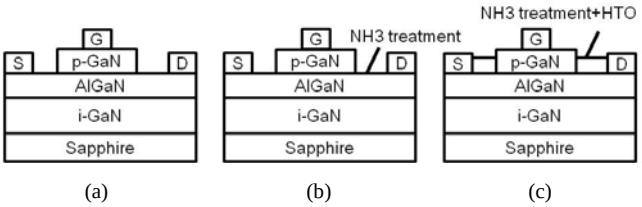

Fig. 1. The schematic of cross section of the devices. (a) no treatment. (b) NH_3 treatment, and (c) NH_3 treatment and HTO passivation layer.

Current collapse measurements

Current collapse of p-GaN gate devices was measured by the following two methods. One is DC and the other is pulse measurement. In DC current collapse measurement, the drain stress voltage was applied under the gate off state after the V_g-I_d measurement. After that, at once, the V_g-I_d characteristics were measured again under the gate on state. The response time is less than 1s from the end of the drain stress voltage to the beginning of the 2nd V_g-I_d measurement. The values of current collapse were obtained from the ratio of R_{ON} (bias-stress) and R_{ON} (unstressed), which were calculated from I_d at V_g=5V of 2nd and 1st V_g-I_d measurements, respectively. The drain stress voltages were 100, 200 and 300V, and the drain stress duration is 10s under gate off voltage of -5V.

In pulse current collapse measurement, the device and load resistance were connected in series and read the value between drain and source voltage V_{DS} of the device using an oscilloscope after the end of drain stress voltage. The operation point of the devices in V_g-I_d characteristics was determined by the value of load resistance. We read the voltage at 10^{-5}s after the end of the drain stress, and calcu-

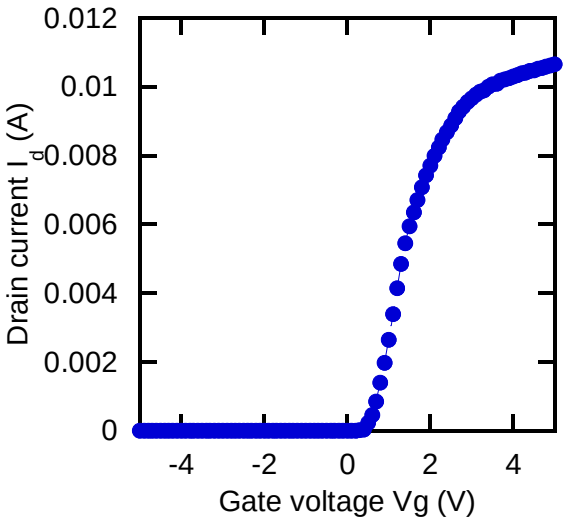

Fig. 2. The V_g-I_d characteristic of device (c) shown in Fig.1. The threshold voltage V_{th} is 0.4V.

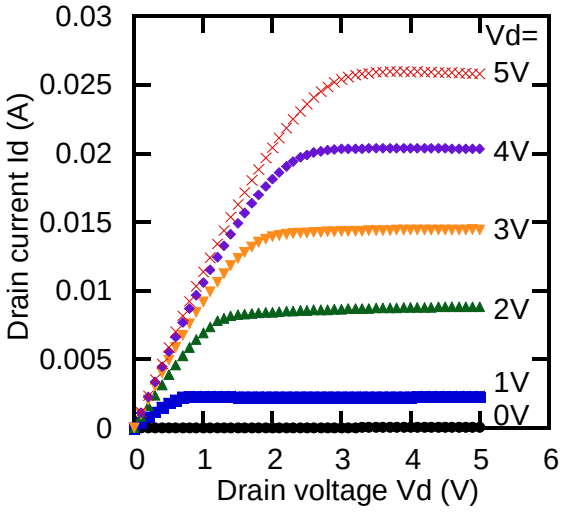

Fig. 3. The V_d-I_d characteristic of device (c) shown in Fig.1. The on resistance Ron is 14 mΩcm^2.

lated the resistance R_{ON} (bias-stress) at the time. It takes the long time to recover the initial state R_{ON} (unstressed). The values of pulse collapse were obtained from the ratio of R_{ON} (bias-stress) and R_{ON} (unstressed). The drain stress voltages were applied at 100, 200 and 300V, and the drain stress duration is 10 s under gate off voltage of -5V.

3. Results and discussion

Fig. 4 shows the current collapse of p-GaN gate devices on the drain stress of 200V. In DC collapse measurement, the values of devices (a), (b) and (c) are 6.4, 1.6 and 1.1, respectively. The values are slightly improved by the effects of NH_3 treatment and HTO passivation layer. On the other hand, in pulse collapse measurement, the values were dramatically decreased by the NH_3 treatment and HTO passivation layer. The values of (a), (b) and (c) are 93, 63 and 12, respectively. It is clear that the current collapse improve the NH_3 treatment and HTO passivation layer. The NH_3 treatment would cause the incorporation of nitrogen into

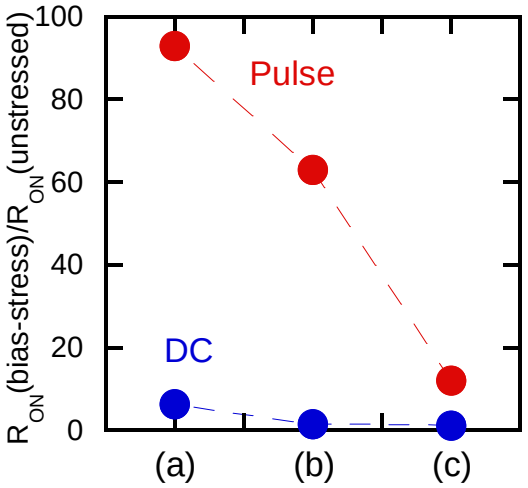

Fig. 4. Dependence of current collapse of p-GaN gate devices (a)~(c). (a) no treatment. (b) NH_3 treatment, and (c) NH_3 treatment and HTO passivation layer

nitrogen vacancies in AlGaN layer. HTO layer would have low fixed defect level material [6]. The values between DC and pulse are different, because the detection time of R after the end of drain stress are extremely different. In other word, the current collapse strongly depends on the time, because some traps with different emission time from the occupied states at the trap levels would be related to the current collapse. Thus, some traps at the surface/interface states, not single trap, causes the current collapse. The device (c) in pulse collapse is 12, which value is not small. However, we think the value will be decreased by the optimum treatment and HTO post-annealing condition.

4. Conclusions

In order to study the relation between surface damage and current collapse, the effects by the surface treatment and passivation layer on the p-GaN gate devices were investigated. The current collapse of DC and pulse were decreased by the NH_3 treatment and HTO passivation layer. The improvement of surface/interface caused the low current collapse of p-GaN gate devices.

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