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Enhancement mode AlGaN/GaN MIS-HEMTs using optimized Si_3N_4 gate insulator

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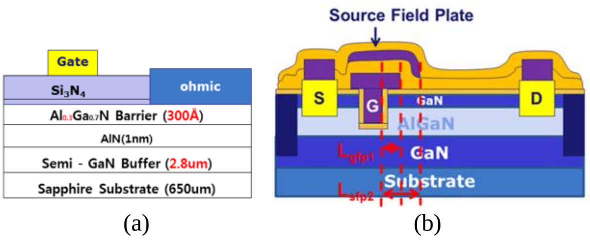
1. Introduction

Because of their superior material properties, GaN based electron devices are very attractive candidates for high power applications [1]. AlGaN/GaN high electron mobility transistors (HEMTs) structures have extremely high electron density at interface, which effectively decreases the on-state resistance, thus reduces the loss of power [2]. This 2DEG channel makes it normally-on devices, for power electronics applications, however, normally-off operation is strongly required to simplify the design of driving circuit [3]. A common method for making normally-off operation is a recessed gate MIS-HEMT. In this study, we employed optimized Si_3N_4 for the gate dielectric by various wet chemical, refractive index of dielectric, and post-deposition annealing to obtain a low on-resistance and high threshold voltage.

2. Optimization of Gate Insulator Characteristics

To evaluate gate insulator characteristics, we used Metal Insulator Semiconductor (MIS) capacitor structures in Fig. 1(a). First, the samples were cleaned by acetone/methanol/IPA, and then various wet chemical treatment which are buffered HF (1:7, 10 min), diluted HF (1:10, 10 min), and aqua regia (1min) were performed. The next series experiments involved different refractive index of Si_3N_4 film. The values of refractive index were 1.95, 2.00, 2.06, and 2.10 respectively. Lastly, post-deposition annealing was split with 600 °C, 700 °C, 800 °C, and 900 °C.

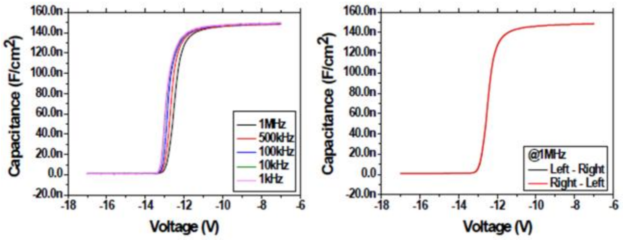
Characteristics of these various MIS capacitor were evaluated by capacitance voltage (CV) hysteresis, frequency dispersion, and leakage current. Wet chemical treatment, refractive index, and post-deposition annealing were very effective to reduce frequency dispersion, hysteresis, and leakage current, respectively. Since wet chemical treatment can remove residues such as carbon, and oxygen [4]. So this process reduces well boarder traps which are related



(a) (b)

Fig. 1 Cross-sectional schematic of (a) MIS capacitor and (b) recessed AlGaN/GaN MIS-HEMTs.

with frequency dispersion [5]. In fact, diluted HF treated sample has lowest frequency dispersion between 1kHz to 1MHz. And the sample of 2.03 refractive index has lowest leakage current, and finally 800 °C post-deposition annealing makes it almost no hysteresis. Characteristics of the optimized MIS capacitor are shown in Fig. 2.



(a) (b)

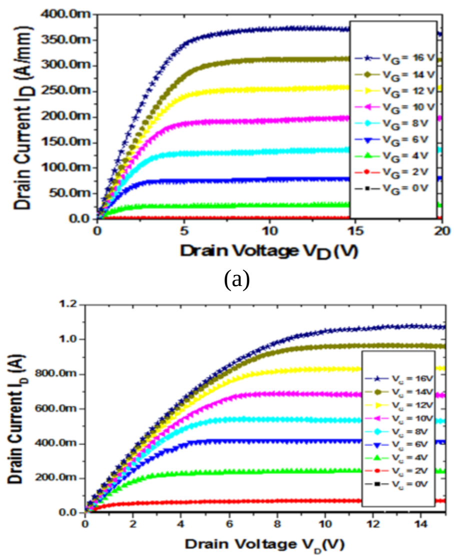
Fig.2 Optimized MIS capacitor CV characteristics of (a) frequency dispersion and (b) hysteresis

3. Device Fabrication and Results

Applying the above high quality MIS condition results, gate recessed enhancement mode AlGaN/GaN MIS-HEMTs were fabricated. The schematic cross section of the proposed AlGaN/GaN recessed gate MIS-HEMT is shown in Fig. 1(b). The epitaxial structure consisted of a 4 nm undoped GaN capping layer, a 20 nm undoped $Al_{0.23}Ga_{0.77}N$ barrier, a 1 nm AlN spacer, a 1.7 µm undoped GaN buffer, and undoped GaN/AlGaN/AlN transition layers on an n-type Si (111) substrate.

First part of the processes was device isolation followed by gate recess using low damage BCl_3/Cl_2 etching by ICP etcher and the targeted etch depth was 19 nm. After that, diluted HF 1:10 cleaning for 10 minutes were performed at the surface, and before dielectric deposition, in-situ vacuum annealing was carried out at 350 °C for 1 hour under a pressure of $\sim 5\times10^{-8}$ torr. And then 30 nm Si_3N_4 with refractive index of 2.03 was deposited by ICP-CVD. For the ohmic contact formation, Si/Ti/Al/Mo/Au (=5/20/60/35/50 nm) metal stack was used and annealed by a RTA at 800 °C for 30 s in nitrogen ambient. A Ni/Au (=20/380 nm) was used for gate metallization with the first gate field plate (L_{gfp1}) length of 2 µm. And 200 nm Si_3N_4 passivation film was deposited at 190 °C. Ni/Au (=20/180 nm) was used to make the 3 µm second source field plate (L_{sfp2}), and finally 300 nm Si_3N_4 was deposited.

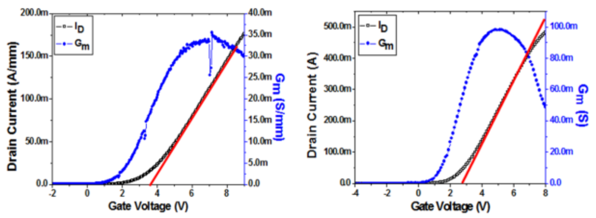
The current-voltage characteristics of devices are in



(a)

(b)

Fig. 3 Current-voltage characteristics of (a) 100µm width unit device and (b) 500µm×7 fingers (total 3.5mm) large device.



(a) (b)

Fig. 4 Transfer characteristics of (a) unit device and (b) large size device in saturation region.

Figs. 3(a) and 3(b). The maximum drain current density of the unit device was 370 mA/mm and maximum drain current of multi-finger device was 1.08 A. The threshold voltages of the fabricated devices were 3.88 V for unit device, and 2.63 V for large device according to linear extrapolation method. Under these conditions, maximum g_m was 35.5 mS/mm for unit device. On-resistance (R_{on}) was calculated using drain current when gate voltage of 16 V and drain voltage of 2.6 V. The value of R_{on} were 3.03 mΩ·cm^2 for unit device, and 3.97 mΩ·cm^2 for large device. The off-state breakdown in Fig. 5 was measured for large size power device with gate voltage of 0 V, and the breakdown voltage of 540 V was achieved.

Results of the above experiments are remarkable. Many researchers have attempted to fabricate enhancement mode. Fig. 6 illustrates the comparison of I_{Dmax} values according to threshold voltage. Most of data was achieved on engineered epi layer, but epi layers used in these experiments utilized conventional structures. In this experiment, however, high performance devices were successfully fabricated without any epi engineering.

Characteristics of the fabricated large size devices were excellent. However, compared to unit device, drain current density and threshold voltage are lower. Even with conditions for high quality dielectric required by MIS-HEMT established, ongoing gate recess process will alter the surface characteristics, so drain current density

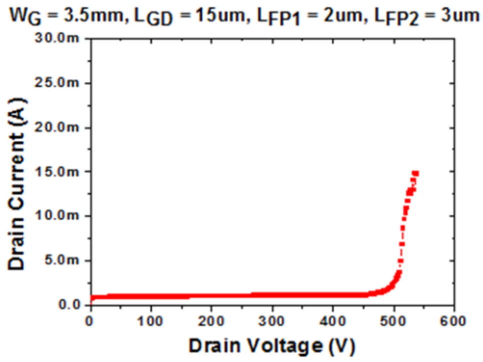


Fig. 5 Breakdown voltage characteristics of multi-finger large size device.

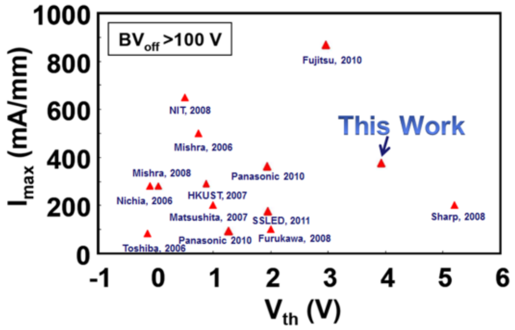


Fig. 6 Performance comparison of I_{Dmax} VS V_{th} with previously reported data.

reduction and on-resistance increase were appeared, and etching non-uniformity maybe lowers threshold voltage.

4. Conclusions

We have demonstrated high quality MIS optimization and high performance multi-finger enhancement mode AlGaN/GaN MIS-HEMTs. The maximum current of ~1.08 A with the threshold voltage of 2.63 V and the breakdown voltage of 540 V were achieved. These results suggest the great potential of our proposed gate recessed AlGaN/GaN MIS-HEMT for high power applications.

Acknowledgements

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References

[1] W. Saito, et al., IEEE Trans. Electron Devices, 53, (2006) 356.
[2] O. Ambacher, et al., J. Appl. Phys, 85 (1999) 3222.
[3] T. Oka, et al., IEEE Electron Device Letters, 29, (2008) 668.
[4] M. Diale, et al., Applied Surface Science, 246, (2005) 279.
[5] M. Fleetwood, et al., Microelectron. Reliab., 35, (1995) 403.