

SiC Vertical Power JFETs for Efficient Power Switching

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1. Introduction

Field effect transistors were among the first transistors invented. Japan has a long history in the development of fundamental theory and operation of field effect transistors (FETs). After the work of Shockley, it was the work by Nishizawa and Watanabe in 1950 that led to the invention of the static induction transistor (SIT) [1-2]. The key design feature of the SIT was the short channel that reduced the current saturation effects and would enable high-frequency and high power operation.

Although the SIT would later be manufactured for many years in Japan for a wide range of power applications, these short channel SITs that are suitable for high frequency operation, were not sufficient for power switching due to the normally-on operation with low blocking capability. The attempt to create a high-voltage JFET with either buried gates [3] or planar structures with deep trenches to enhance the blocking gain [4] were somewhat successful, but ultimately were never commercialized on a large scale. With the invention of the SCR by GE in 1957 [5], and the VMOSFET by Nishizawa and Watanabe, much of the focus for power devices was turned to the safety and power handling capability of bipolar and MOS based power devices.

Now over 50 years later, the material advancements in bulk SiC have enabled the resurrection of a high voltage JFET technology that can achieve a high blocking gain normally-off or normally-on operation while providing switching speeds exceeding state of the art Si technologies.

2. SiC JFET: Static Characteristics

Table I gives the fundamental material parameters for several of the most promising semiconductor materials. The advantage for SiC in creating a normally-off JFET is the wide bandgap compared to Si. In order to create a normally-off JFET there are two main criteria that must be met; 1) a long channel for high voltage gain for good

Table I Comparison of key semiconductor material parameters

	Si	GaAs	GaN	4H-SiC
E_g (eV)	1.1	1.5	3.4	3.3
μ_n (cm ² /V·s)	1350	8500	≤ 1000	≤ 900
v_{sat} (cm/s)	1×10 ⁷	1×10 ⁷	2×10 ⁷	2×10 ⁷
E_{crit} (V/cm)	1×10 ⁵	4×10 ⁵	5×10 ⁶	3×10 ⁶
κ (W/cm·°C)	1.5	0.5	1.3	3.7

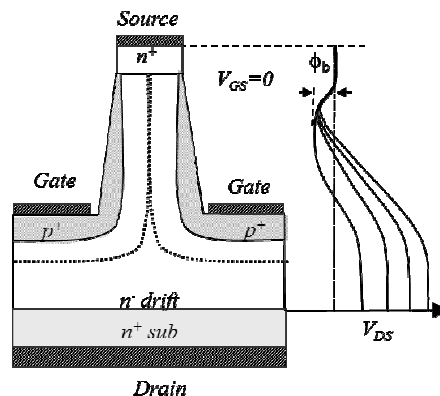


Fig. 1 Schematic cross section of a SiC trench JFET unit cell showing the long channel with a potential barrier that can withstand high reverse bias.

blocking capability, and 2) a threshold voltage and transconductance such that high current can be sourced without excess injection from the controlling gate diode. Fig. 1 shows a cross section of the unit cell structure of the normally-off JFET with a long channel able to withstand high reverse voltage without significant reduction in the channel barrier potential. Si devices can also create a normally-off structure, but the high critical field strength of SiC (10X Si) allows for much higher voltage operation before drain induced barrier lowering (DIBL) causes excess leakage currents.

The second advantage the high bandgap of SiC pro-

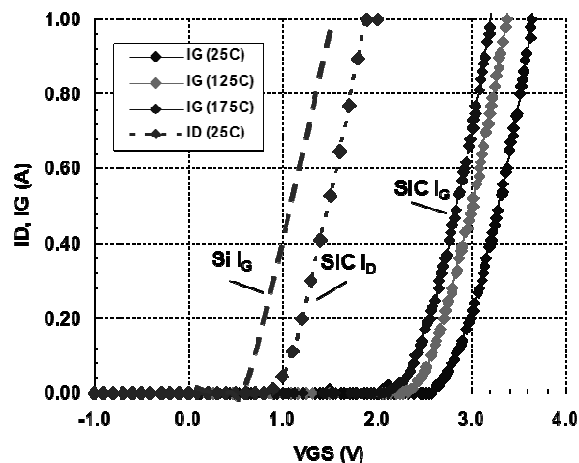


Fig. 2 SiC JFET transfer and gate IV curves showing the margin between device threshold and injection of the gate diode.

vides for normally-off operation is the reduction of minority carrier injection current during on-state operation. Fig. 2 illustrates the voltage margin available for SiC compared to Si. To maximize the noise margin, the threshold voltage (V_{TH}) needs to be appreciably higher than 0V. For SiC devices, the typical V_{TH} is $\sim 1V$. For a Si device, this would cause excess minority carrier injection from the gate-source diode due to the low V_{bi} of 0.7V. In SiC, however, no injection occurs until the gate bias exceeds the considerably higher V_{bi} of $\sim 3V$.

The long channel device is optimized to keep the drain from punching through to the source in blocking mode. Fig. 3 shows the DIBL characteristic for a normally-off trench JFET with a threshold voltage of $\sim 1V$. These characteristics demonstrate the threshold voltage change and leakage current increase with increasing drain-source voltage versus applied V_{GS} . With this design, the JFET remains in the off state with less than 0.1uA of drain leakage for a $V_{DS}=1000V$ and $V_{GS}=0V$.

The output I-V characteristics are given in Fig. 4. The vertical structure and lack of MOS channel gives the JFET the lowest reported specific $R_{DS(ON)}$ values of any power transistor available on the market today [6]. For the 50m Ω rated device in Fig. 4, the $R_{DS(ON),sp}$ is only 2.4m Ω -cm², with an output current > 50A in the fully enhanced state.

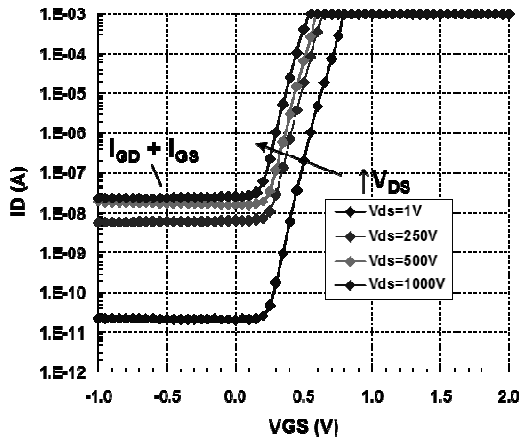


Fig. 3 DIBL characteristics of a 1200V trench JFET.

3. AC Performance

Due to the small die size and unipolar nature, the switching performance is excellent. Fig. 5 gives the switching energy measurements of a 100m Ω trench JFET vs load current and temperature. At $I_D=10A$, the total switching energy is less than 150uJ, which is $\sim 10X$ smaller than a similarly rated 1200V Si IGBT. Additionally, because it is a pure unipolar device, the switching energies are independent of temperature.

3. Conclusion

With the material advantages of SiC, a power trench

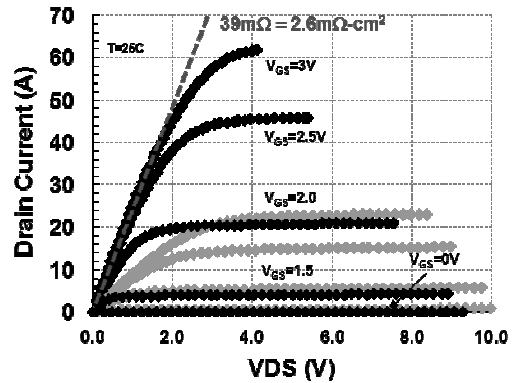


Fig. 4 Output characteristics of a 50m Ω trench JFET.

JFET technology is now able to provide nearly a 10X advantage over existing Si power devices. Both normally-on and normally-off devices are possible, each with distinct advantages to the circuit designer. Application examples such as 99% solar inverter efficiency, new short circuit protection methods, and high temperature power modules will be presented.

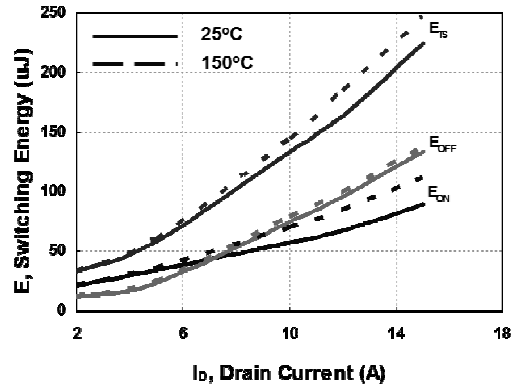


Fig. 5 Measured switching energy of a 100m Ω SiC trench JFET vs. drain current at $V_{DS}=600V$.

References

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