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600-V 27-mΩ Normally-off SiC JFET for High Efficiency Power Supply

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1. Introduction

Silicon-carbide (SiC) junction field effect transistors (JFETs) have been developed for next generation high-power devices [1] preceding SiC MOSFETs, because they have no oxide/semiconductor interface in the channel region, which causes both gate oxide break-down and threshold voltage variation of SiC MOSFETs [2]. Given this advantageous feature of JFETs, authors previously developed 600-V normally-off JFETs for enhancing current density by optimizing the impurity profile near the p-n junction between the gate region and the channel region [3]. However, these previously developed JFETs are not suitable for high-power applications such as high-efficiency power supplies and hybrid electric vehicles because of their insufficient blocking voltage of about 600 V. In addition, large gate leakage current in the JFETs causes large power loss in gate driver circuits, and the small size of JFETs (namely, 2.0 mm□) limits driving current to less than 10 A.

In the present study, to address the above-described issues, we attempted to increase the blocking voltage of JFETs by localized current-path doping (LCD) and to reduce their inherent gate leakage current by surface oxynitridataion (SON). We fabricated 3.9-mm□ low on-resistance JFETs for a high-efficiency power supply, and we estimated the effect of reducing power loss under the assumption that the proposed JFETs are utilized for a power supply.

2. Experimental

A schematic cross-sectional view of the proposed JFET structure is shown in Fig. 1(a). The substrate is an n-type 4H-SiC wafer containing an 8-μm-thick n-type epilayer with a doping level of 2.0×10^{16} cm^{-3}. The p- termination region and the n+ source region were selectively implanted with lithography and dry etching. A gate trench was formed with dry etching, followed by ion implantation for the p+ gate region. Additionally, localized current-path doping (LCD) of nitrogen was performed to widen the effective current path without degrading blocking voltage. After activation annealing at 1800° C, to decrease the gate leakage current, surface oxynitridation (SON) was performed at 1300° C in nitric oxide (NO) ambient instead of conventional dry oxidation at 1150° C. Ohmic contacts of the source, gate and drain were then formed with nickel-titanium silicide. Finally, a SiO2 interlayer and aluminum electrodes were formed. Active sizes of fabricated JFETs are 3.9 × 3.9 mm. For investigating reduction of gate-leakage current by SON, smaller JFETs with a size of 1.1 × 1.1 mm were also fabricated. As shown in Fig. 1(b), gate pads are located at the center of the JFET chips to decrease internal gate resistance. *I-V* characteristics of the JFETs were measured with Agilent B1505A power device analyzer. On the basis of efficiency of an existing server power supply and the measured *I-V* characteristics, loss of server power supply was then estimated.

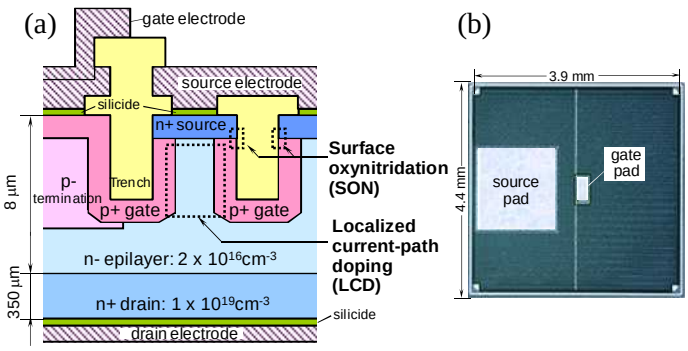

Fig. 1(a) Schematic cross-sectional view of proposed SiC JFET fabricated by localized current-path doping (LCD) and surface oxynitridation (SON). (b) Photograph of proposed SiC JFET.

3. Results and discussion

Dependence of drain current density on break-down voltage BV_{DSS} of a fabricated 3.9-mm□ JFET and that of a previous work are plotted in Fig. 2. In the previous work, current-path doping was also applied to reduce channel resistance. However, n-type dopants were excessively doped at the bottom of the p+ trench gate when the conventional doping technique was used. According to electric-field analysis by a device simulator (Fig. 3), the electric field at the bottom of the gate is thus increased from 0.9 to 1.7 MV/cm. As shown in Fig. 2, in the previous work, an

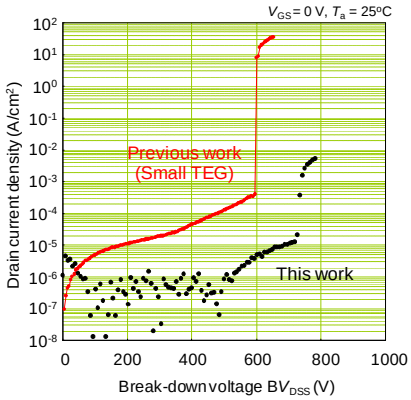

Fig. 2 Dependence of drain current density on break-down voltage BV_{DSS}.

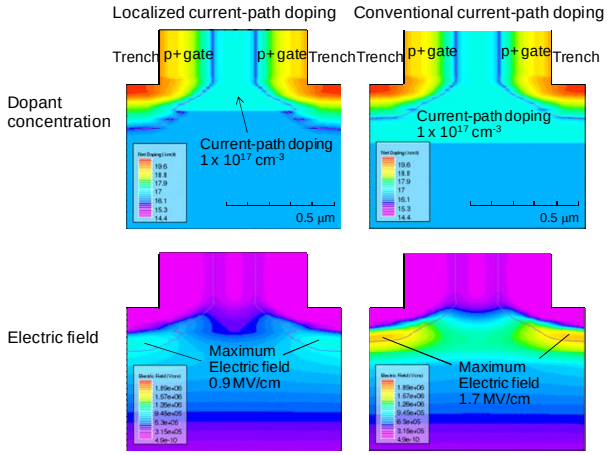

Fig. 3 Simulated results of electric field at bottom of trench.

avalanche breakdown is caused at blocking voltage of 600 V. On the other hand, when the proposed localized current-path doping (LCD) was used, to avoid the avalanche break-down, the n-type dopants are only doped between the p+ gate and the n-channel (Fig. 1(a)). Blocking voltage therefore becomes over 700 V without negative gate bias.

Dependence of gate current on gate voltage of the 1.1-mm□ JFETs is plotted in Fig. 4. It is well known that the oxide/SiC interface formed by dry oxidation has many surface defects [2]. Moreover, the proposed JFET structure has a p-n junction between the p+ gate and the n+ source with a large perimeter. It is therefore considered that a large part of the gate current is generated by mediation at the surface defects. The gate leakage current is reduced by passivation of the surface defects by surface oxynitridation (SON). The gate leakage current of the fabricated 1.1-mm □ JFETs is shown in Fig. 4. It is clear from the figure that the gate leakage current was significantly decreased, namely, by about one tenth by SON.

Dependence of drain current on drain voltage of the JFETs is plotted in Fig. 5.According to these plots, on-resistance at 25°C is 27 mΩ and that at 125°C is 38 mΩ . In general, on-resistance is proportional to T^n, where T and n represent absolute temperature and power factor, respectively. Here, n of the fabricated JFETs is 1.1 which is much smaller than that of silicon super-junction MOSFETs (SJ-MOSFETs), 2.7 [4]. This difference between n values means that SiC JFETs have an advantage especially in regard to high-temperature operation over silicon SJ-MOSFETs, which are applied as power switches in many power supplies. It is due to difference between the electron scattering mechanisms of JFETs and silicon SJ-MOSFET, which directly affect electron mobility. In the case of low dopant concentration, electron mobility is mainly affected by phonon scattering leading to an n value larger than two. On the other hand, in the case of high dopant concentration, electron mobility is mainly affected by ionized impurity scattering leading to an n value lower than zero. Since dopant concentration of the channel region (formed by LCD) of the developed JFETs is higher than that of the epilayer, the n value of the JFETs is considered to be low.

According to the above-described measured characteristics of JFETs, power loss in a server power supply due to application of JFETs was estimated, as shown in Fig. 6. Power loss of FETs in power factor correction (PFC) and DC/DC inverter circuits can be decreased by 66-% by means of replacing silicon MOSFETs with SiC JFETs with low on-resistance and low gate leakage current.

4. Conclusions

Normally-off SiC JFETs with high blocking voltage and low gate leakage current were fabricated by localized current-path doping (LCD) and surface oxynitridation (SON). Applied in a server power supply, these improved JFETs (with on-resistance of 27mΩ) were estimated to decrease power loss due to FETs by 66 %.

Acknowledgements

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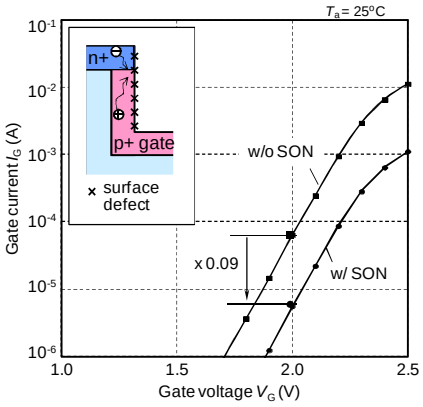

Fig. 4 Dependence of gate current I_G on gate voltage V_G.

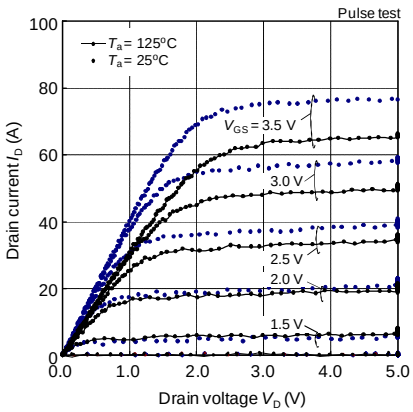

Fig. 5 Dependence of drain current I_D on drain voltage V_D.

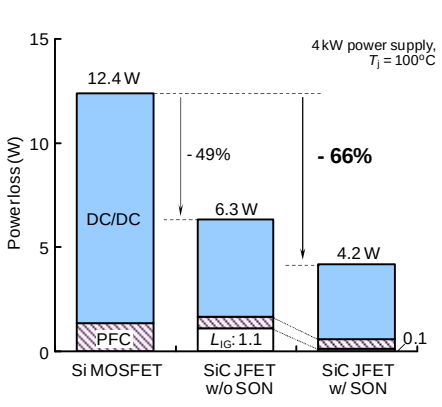

Fig. 6 Calculated power loss of FETs in power factor correction (PFC) and DC/DC inverter circuits.