Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials, Kyoto, 2012, pp895-896

Lateral High-Voltage 4H-SiC IGBTs

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1. Introduction

Due to the unique properties such as wide band gap, high breakdown field, and high saturation velocity, silicon carbide is suitable for high-temperature, high-power, and high-frequency applications. For high-voltage applications, it is desirable to use a bipolar device to reduce the conduction loss because of the conductivity modulation in the long drift region. In this paper, a 4H-SiC lateral high-voltage n-channel IGBT on a semi-insulating substrate is demonstrated. Various process improvements, such as N_2O annealing, lifetime enhancement, were conducted in order to obtain better forward characteristics. The temperature dependence of the device characteristic was also investigated. The differential on-resistance exhibits an negative temperature dependence, whereas the common base current gain α_{pnp} of the parasitic pnp BJT have a complicated temperature dependence because it is affected by carrier mobility, carrier lifetime, and the ionization percentage of the p+ collector.

2. Device Structure and Experiment Result

Device Structure

The proposed lateral IGBT, as shown in Fig. 1, was fabricated on a p-type epilayer on a 4H-SiC semi-insulating wafer with an n-buffer layer placed between p+ collector and p epilayer to prevent vertical punch-through. Tab. 1 summarizes the structures and process parameters of three devices to be compared. Different drift region lengths L_d = 20, 40, 80 μm, were used. By comparing the devices, the influences of lifetime and the doping of n-buffer dose, which affects the injection efficiency of p-collector, will be examined. The p-epilayer is $2\mu m/5\times10^{16} cm^{-3}$. The drift region was formed by implantation of nitrogen with doses of 1×10^{13} cm^{-2} into p-type epilayer. Emitter and collector were made by implantation of phosphorus and aluminum at 650 °C, respectively. Following the implantation and mesa trench isolation, a two-step lifetime enhancement process proposed by reference [1] was carried out. First, by thermal oxidation of 4H-SiC at 1150 °C for one hour, followed by an additional annealing in Ar at 1700 °C for 10 minutes. Activation for all implanted species was also completed at the same time. Thus, the concentrations of the major deep levels are expected to reduce with the two-step thermal treatment, resulting in an improvement of carrier lifetime. Graphite cap was used during annealing to preserve good surface morphology. After RCA clean, a 700 Å gate oxide was deposited, followed by an N_2O annealing. Contact metal consisting of 20 nm Ti and 100 nm Ni was used for the n+ contact. A layer of 20 nm Ti, 120 nm Al, and 100 nm Ni was employed for the p+ contact. Then, a rapid thermal annealing was done at 1150 °C for 3 minutes in vacuum to sinter these contact metal. Ti/Al of 20 nm/350 nm was deposited and lifted off to form gate electrode. Finally, both contact and gate metal was covered by a pad metal composed of Ti/Al of 20 nm/480 nm for probe testing.

Experiment Results

The channel mobility are measured at a V_{ds} of 0.1 V from a test MOSFET with channel length L_{ch} = 100 μm. The measured field effect mobility at room temperature is 25 cm^2/Vs. Fig. 2 illustrates the on-state and blocking characteristic of an IGBT with W = 842 μm, L_{ch} = 5 μm, L_d = 80 μm, as shown in the inset in Fig. 2. The device shows a threshold voltage of 2.9 V. The specific differential on-resistance extracted at V_g = 30 V and V_{ce} = 4 V is found to be 425 mΩ-cm^2 and the breakdown voltage is 2670 V at a current exceeds 10 μA. Fig. 3 shows the saturation collector current ($I_{c,sat}$) and saturation transconductance ($g_{m,sat}$) of an IGBT with L_d of 20 μm as a function of gate bias. It is clear that both $g_{m,sat}$ and $I_{c,sat}$ of IGBT are increased by the parasitic BJT with a factor of $(1-\alpha_{pnp})^{-1}$[2], compared to its MOSFET counterpart. The α_{pnp} is estimated to be 0.31 at a V_{ce} of 100 V and a V_g of 20 V. The forward I-V characteristic of IGBT and MOSFET at 200 °C is illustrated in Fig. 4. Fig. 5 compares the differential on-resistance of a MOSFET and an IGBT at a V_g of 30 V at room temperature and 200 °C. The differential on-resistance exhibits a negative temperature dependence. At room temperature, the differential resistance of IGBT is lower than that of MOSFET when I_c is larger than 15 mA, indicating the injection of minority carriers. The crossover current is reduced to 3.7 mA at 200 °C, which is attributed to the increase in minority carrier lifetime in drift region at high temperatures. From the measurement results, a device with a lower doping buffer (better injection efficiency), a shorter base and an increased lifetime (better base transport factor) has the highest α_{pnp} among all the conditions. α_{pnp} has a small and complicated temperature dependence because the important factors such as the carrier lifetime, the carrier mobility, and p+ collector have different temperature dependence .

3. Conclusion

Lateral high-voltage 4H-SiC IGBTs are fabricated and characterized. The specific differential on-resistance is 425 mΩ-cm^2 and the breakdown voltage is 2670 V for a device with 80 μm drift region. Drift region length, buffer doping, and lifetime improvement are important for the parasitic BJT's function. With a better design, the differential on-resistance of an IGBT can be lower than that of a MOSFET, and is further reduced at higher temperatures.

Acknowledgement

This work is supported by National Science Council of Taiwan, R. O. C. under Contract No. 100-2221-E-007-025 and No. 99-2221-E-007-122

References

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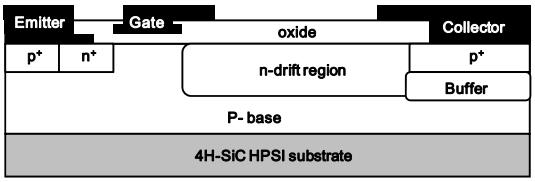

Fig. 1 Lateral 4H-SiC IGBTs on a semi-insulating substrate

Group name / parameters	Buffer dose(cm^{-2})	Lifetime improvement	Channel length(μm)	Single-zone drift region(μm)		
IGBT 1	Lighter 3x10^{13}	Yes	5	20	40	80
IGBT 2	Lighter 3x10^{13}	-	5	20	40	80
IGBT 3	Heavier 6x10^{13}	Yes	5	20	40	80

Tab. 1 Structures and parameters of lateral IGBTs with different designs

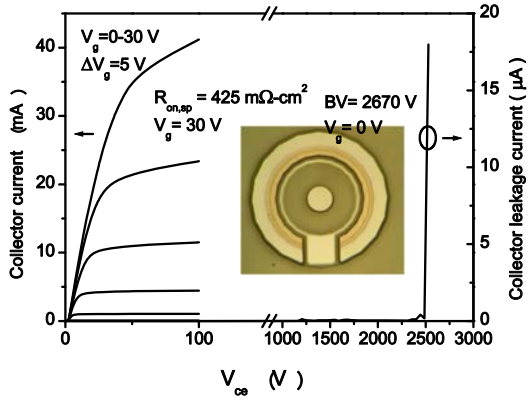

Fig.2 Forward and blocking characteristics of a lateral IGBT (group IGBT1) with L_{ch} of 5 μm and L_d of 80 μm. The inset shows the photograph of the fabricated IGBT.

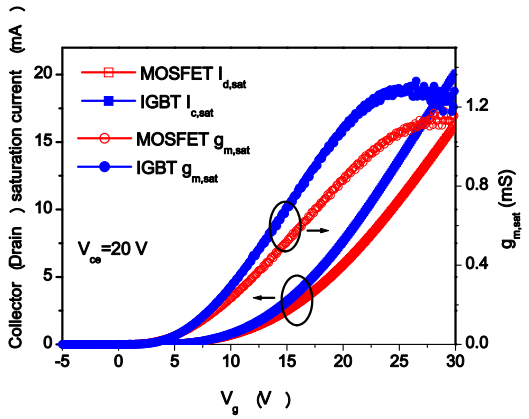

Fig.3 Comparisons of $I_{c,sat}$ and $g_{m,sat}$ versus V_g between an IGBT (group IGBT1) and a MOSFET with a L_{ch} of 5 μm and a L_d of 20 μm.

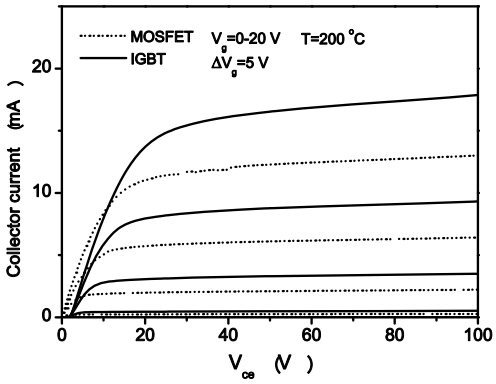

Fig.4 I-V characteristics of an IGBT (group IGBT1) and a MOSFET with an L_d of 20 μm at 200 °C.

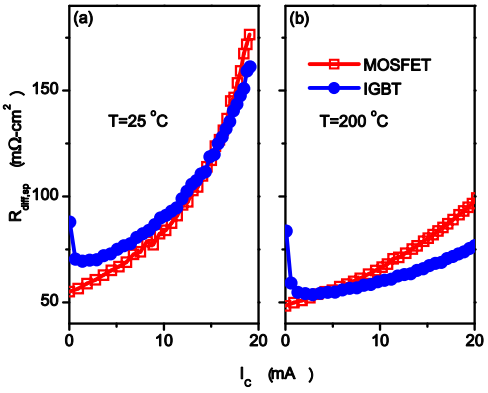

Fig. 5 The differential on-resistance of a MOSFET and an IGBT at a V_g of 30 V (a) at room temperature and (b) at 200 °C.