Significant Effect of JFET Doping on Low On-resistance
4H-SiC DMOSFETs of 3300 V Rating

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1. Introduction
SiC power devices have so far been researched and developed mainly for middle-voltage classes [1-3]. Recently, their research field has expanded to higher power inverter/converter systems, which support society’s infrastructures, such as electric power industries and railways. We have reported development of hybrid power modules with 1700V-class SiC Schottky barrier diodes for traction inverters [4]. In the applications described above, power switching devices handling even higher voltage have also been demanded. Therefore, in this paper, 3300V-class SiC breakdown voltage. A 50-nm thick gate oxide was formed by thermal oxidation with subsequent nitridation. All the forms an
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2. Device Structures
Fabrication of doubly-implanted vertical MOSFETs was performed on 4Hn-SiC (0001) wafers with a 30 µm lightly-doped n-type drift layer (ND−NA = 3.0×1015 cm−3). An originally-developed field limiting ring structure was employed for the junction termination which guarantees stable avalanche breakdown at around 4 kV. JD was performed with multiple high-energy nitrogen implantation to form an n+ layer. The doping condition was carefully
designed in advance by process and device simulations since it significantly influences both the on-resistance and the breakdown voltage. A 50-nm thick gate oxide was formed by thermal oxidation with subsequent nitridation. All the devices fabricated in this study consist of several tens of square-shaped unit cells arranged with a cell pitch (Lcell) of 11 µm.

3. Results and Discussion
Figure 1 shows the temperature dependence of the specific on-resistance (Ron,sp) on the channel length (Lch) of MOSFETs fabricated with and without the JD process. Their JFET length (LJ) is 3.0 µm, and the data were taken at room temperature. Ron,sp decreases monotonically as Lch is short-
length.

Figure 2 shows the L1 dependence of Ron,sp. Ron,sp increases drastically for short L1, and this increase occurs at a longer L1 in the devices without JD. Since Ron,sp of the devices with JD is smaller than that without in the entire L1 range studied here, the effect of the depletion layer in the JFET region as well as the spread resistance are supposed to be influential on Ron,sp. Figures 3(a) and 3(b) show an analysis of the resistive components of Ron,sp with and without JD, respectively. The normalized resistances of the drift, JFET, and channel regions (Rd, Rdif, and Rch) were estimated by TEG (Test Element Group) analyses. Rch is decreased by shortening L1 regardless of the application of the JD process, and this is due to the increase of the channel width density while Ladj and LFP are both kept constant. Besides, Rd+Rdif increases significantly as L1 is shortened, and the effect is more pronounced in the devices without JD. This result suggests that lowering Rd+Rdif is quite effective in reducing the MOSFET’s total resistance.

Figure 4(a) shows the L1 dependence of the blocking voltage between the source and the drain electrodes (BVDS) at VGS = −10 V. The JD process is seen to lower BVDS as L1 increases. This result indicates that with long L1 the field shielding effect by the depletion layer becomes weaker by the adoption of the JD process. Figure 4(b) shows the simulated results of the L1 dependence of the electric field at the edge of the p-well region (ESiC) at a VDS bias of 3300 V. At long L1 and adoption of the JD process both lead to an increase in ESiC, which affects BVDS. Thus, it is important to select the optimum cell structure for ensuring reliability as both Ron,sp and BVDS decrease with JD.

Figure 5 shows typical JDS-VDS characteristics of the MOSFET with JD having an optimized L1 of 2.2 µm. Ron,sp was deduced to be about 14 mΩcm² at JDS = 100 A/cm². Figure 6(a) shows the temperature dependence of Ron,sp. The MOSFET with JD shows lower Ron,sp and a smaller temperature coefficient at higher temperatures compared
with that without. This result was analyzed using TEG devices and summarized in Figure 6(b) where the temperature dependences of $R_t + R_{\text{drift}}$ and $R_{\text{ch}}$ are shown. The temperature coefficients of $R_{\text{ch}}$ of the two devices were deduced to be almost the same value, since the JD was designed not to affect the channel characteristics. The negative coefficients should be due to the increase in the channel mobility at high temperature. On the other hand, $R_t + R_{\text{drift}}$ increases at higher temperature, and the temperature coefficient is smaller in the devices with JD. This is considered to be because the JFET region with higher doping concentration makes devices less sensitive to temperature in terms of the resistivity. These results suggest that the JFET doping is effective in realizing MOSFETs with low on-resistance at and above room temperature. In this case, short $L_I$ should be employed in terms of the reliability in high voltage environments.

4. Summary

We investigated the effects of JFET doping on the static characteristics of 3300V-class SiC DMOSFETs. The JFET doping technique was revealed to be significantly effective in reducing the on-resistance, especially the JFET resistance, with no degradation in the breakdown characteristics for devices with properly structured unit cells. It is also a favorable technique in terms of lowering the on-resistance at high temperatures where the JFET resistance severely increases.

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References