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Significant Effect of JFET Doping on Low On-resistance 4H-SiC DMOSFETs of 3300 V Rating

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1. Introduction

SiC power devices have so far been researched and developed mainly for middle-voltage classes [1-3]. Recently, their research field has expanded to higher power inverter/converter systems, which support society's infrastructures, such as electric power industries and railways. We have reported development of hybrid power modules with 1700V-class SiC Schottky barrier diodes for traction inverters [4]. In the applications described above, power switching devices handling even higher voltage have also been demanded. Therefore, in this paper, 3300V-class SiC DMOSFETs (Double-diffused Metal-Oxide-Semiconductor Field Effect Transistors) are investigated in detail. Effectiveness of doping into the JFET (Junction Field Effect Transistor) region of a MOSFET (JFET doping (JD)) on realizing low on-resistance was revealed even at high temperatures.

2. Device Structures

Fabrication of doubly-implanted vertical MOSFETs was performed on 4Hn-SiC (0001) wafers with a 30 μm lightly-doped *n*-type drift layer (N_D–N_A = 3.0×10^{15} cm^{-3}). An originally-developed field limiting ring structure was employed for the junction termination which guarantees stable avalanche breakdown at around 4 kV. JD was performed with multiple high-energy nitrogen implantation to form an n^- layer. The doping condition was carefully designed in advance by process and device simulations since it significantly influences both the on-resistance and the breakdown voltage. A 50-nm thick gate oxide was formed by thermal oxidation with subsequent nitridation. All the devices fabricated in this study consist of several tens of square-shaped unit cells arranged with a cell pitch (L_{FP}) of 11 μm.

3. Results and Discussion

Figure 1 shows the dependence of the specific on-resistance ($R_{on,sp}$) on the channel length (L_{ch}) of MOSFETs fabricated with and without the JD process. Their JFET length (L_J) is 3.0 μm, and the data were taken at room temperature. $R_{on,sp}$ decreases monotonically as L_{ch} is shortened, and it shows nearly the same trend regardless of the use of JD process. The smaller $R_{on,sp}$ for the devices with JD is due to the reduction of the JFET resistance. The channel mobility was deduced to be about 22 cm^2/V·s in both structures.

Figure 2 shows the L_J dependence of $R_{on,sp}$. $R_{on,sp}$ increases drastically for short L_J, and this increase occurs at a longer L_J in the devices without JD. Since $R_{on,sp}$ of the devices with JD is smaller than that without in the entire L_J range studied here, the effect of the depletion layer in the JFET region as well as the spread resistance are supposed to be influential on $R_{on,sp}$. Figures 3(a) and 3(b) show an analysis of the resistive components of $R_{on,sp}$ with and without JD, respectively. The normalized resistances of the drift, JFET, and channel regions (R_J, R_{drift}, and R_{ch}) were estimated by TEG (Test Element Group) analyses. R_{ch} is decreased by shortening L_J regardless of the application of the JD process, and this is due to the increase of the channel width density while L_{ch} and L_{FP} are both kept constant. Besides, R_J+R_{drift} increases significantly as L_J is shortened, and the effect is more pronounced in the devices without JD. This result suggests that lowering R_J+R_{drift} is quite effective in reducing the MOSFET's total resistance.

Figure 4(a) shows the L_J dependence of the blocking voltage between the source and the drain electrodes (BV_{DS}) at V_{GS} = −10 V. The JD process is seen to lower BV_{DS} as L_J increases. This result indicates that with long L_J the field shielding effect by the depletion layer becomes weaker by the adoption of the JD process. Figure 4(b) shows the simulated results of the L_J dependence of the electric field at the edge of the *p*-well region (E_{SiC}) at a V_{DS} bias of 3300 V. At long L_J and adoption of the JD process both lead to an increase in E_{SiC}, which affects BV_{DS}. Thus, it is important to select the optimum cell structure for ensuring reliability as both $R_{on,sp}$ and BV_{DS} decrease with JD.

Figure 5 shows typical I_{DS}-V_{DS} characteristics of the MOSFET with JD having an optimized L_J of 2.2 μm. $R_{on,sp}$ was deduced to be about 14 mΩcm^2 at J_{DS} = 100 A/cm^2.

Figure 6(a) shows the temperature dependence of $R_{on,sp}$. The MOSFET with JD shows lower $R_{on,sp}$ and a smaller temperature coefficient at higher temperatures compared

with that without. This result was analyzed using TEG devices and summarized in Figure 6(b) where the temperature dependences of R_J+R_{drift} and R_{ch} are shown. The temperature coefficients of R_{ch} of the two devices were deduced to be almost the same value, since the JD was designed not to affect the channel characteristics. The negative coefficients should be due to the increase in the channel mobility at high temperature. On the other hand, R_J+R_{drift} increases at higher temperature, and the temperature coefficient is smaller in the devices with JD. This is considered to be because the JFET region with higher doping concentration makes devices less sensitive to temperature in terms of the resistivity. These results suggest that the JFET doping is effective in realizing MOSFETs with low on-resistance at and above room temperature. In this case, short L_J should be employed in terms of the reliability in high voltage environments.

4. Summary

We investigated the effects of JFET doping on the static characteristics of 3300V-class SiC DMOSFETs. The JFET doping technique was revealed to be significantly effective in reducing the on-resistance, especially the JFET resistance, with no degradation in the breakdown characteristics for devices with properly structured unit cells. It is also a favorable technique in terms of lowering the on-resistance at high temperatures where the JFET resistance severely increases.

Acknowledgements

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References

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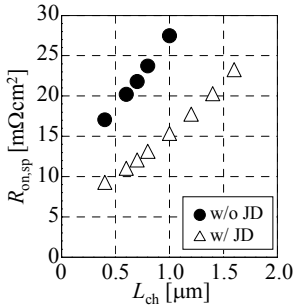

Fig. 1 Dependence of specific on-resistance on the MOSFETs' channel length

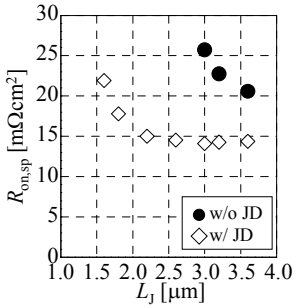

Fig. 2 JFET length dependence of specific on-resistance

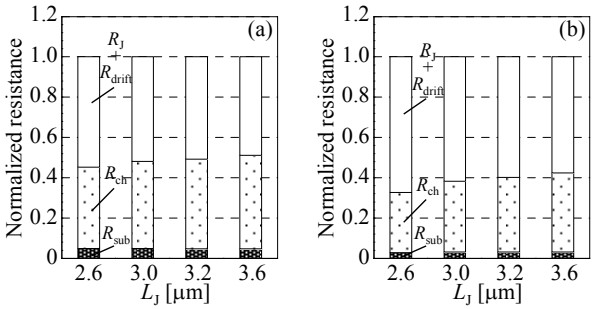

Fig. 3 Analysis of the resistive components of specific on-resistance (a) with JD and (b) without JD

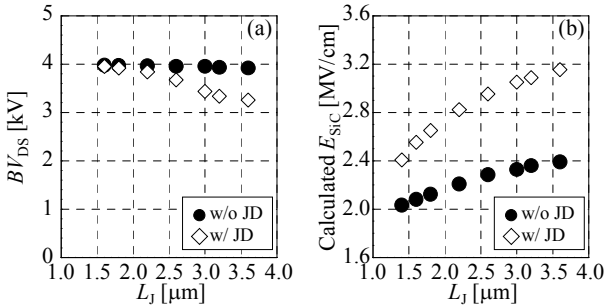

Fig. 4 JFET length dependence of (a) blocking voltage and (b) simulated electric field at the edge of the *p*-well region

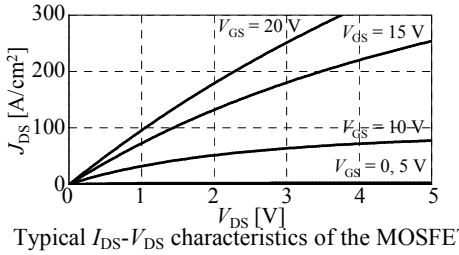

Fig. 5 Typical I_{DS}-V_{DS} characteristics of the MOSFET having the optimized L_J of 2.2 μm with JD

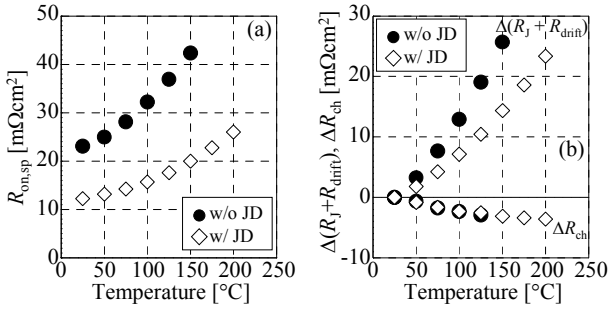

Fig. 6 Temperature dependence of (a) on-resistance and (b) variation of JFET, drift and channel resistances compared with the values at 25 °C