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Advanced SiC Devices with Trench Structure

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1. Introduction

This paper presents next generation Silicon Carbide (SiC) trench structure Schottky diodes, and trench MOSFETs. SiC Schottky diodes, with newly developed trench structures, successfully showed lower forward voltage than conventional SiC diodes while keeping leakage current at an acceptable level. The developed SiC MOSFETs with a double-trench structure have improved reliability of the device while maintaining ultra low on-resistance due to the fact that the new structure effectively reduced the highest electric field at the bottom of the gate trench, preventing gate oxide breakdown.

2. SiC Trench Structure Schottky Diodes

SiC Schottky diodes are attractive devices to reduce switching losses in high voltage applications such as Power Factor Correction (PFC) [1,2]. The reduction of conductive losses is also required to improve efficiency. However, SiC Schottky diodes have higher forward voltage drop when compared to silicon PN junction diodes. We have proposed the trench structure Schottky diodes to obtain a lower forward voltage drop while maintaining the same leakage current. Trench p region can suppress the concentration of electric field at the Schottky interface. The threshold voltage of the trench structure is 0.48 V smaller than that of the planar structure. The smaller threshold voltage can reduce the conductive losses during forward current operation.

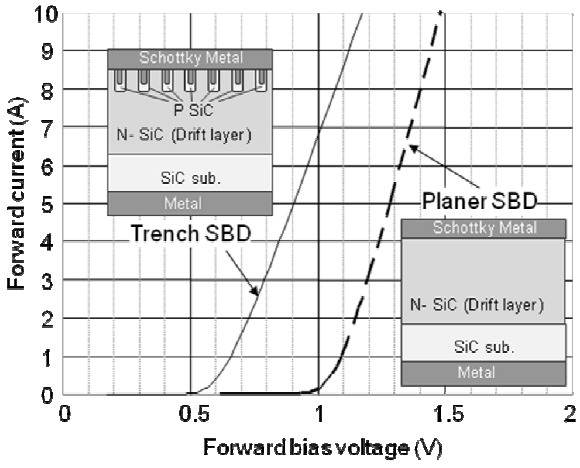

Fig.1 Forward Characteristics of planer SBD and trench SBD

3. SiC Double-Trench MOSFETs

SiC trench MOSFETs can have lower conductive losses when compared with planar MOSFETs because planar MOSFETs have JFET regions which increase the on-resistance [3,4]. We previously reported 790 V SiC trench MOSFETs with the lowest R_{on} at room temperature. However, the trench MOSFETs had issues regarding oxide breakdown at the trench bottom during high drain-source voltage application. To resolve issue of gate oxide breakdown, double-trench MOSFET structure, which has both source and gate trenches, was developed. The device structures for the single and double-trench structures are shown in Fig.2 (a) and (b), respectively.

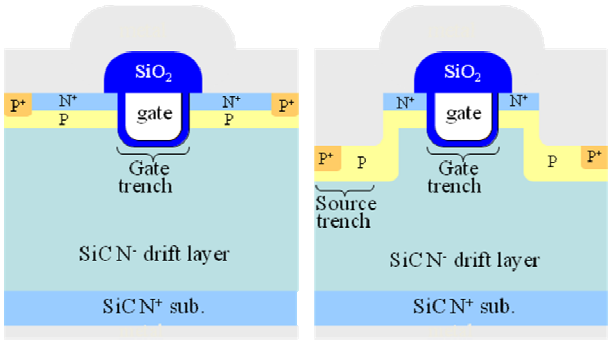

Fig.2 Schematic cross section of (a) conventional single-trench structure and (b) double-trench structure with source trench and gate trench.

To suppress electric field at the gate oxide bottom, the source trench is fabricated deeper than gate trench. Deeper source trenches prevent the concentration of electric fields at the bottom of the gate trench. Fig.3 shows drain-source bias simulation results of the electric field distribution at 600V and with a gate-source voltage of 0V. Epitaxial layers were 7μm thick with a doping concentration of 7.5 x 10^{15}cm^{-3}. The highest electric field at the bottom of the gate trench of the single-trench structure was 2.66 MV/cm. On the other hand, that of double-trench structure was 1.66 MV/cm. This structure succeeds in preventing the destruction of oxide at the bottom of the gate trench.

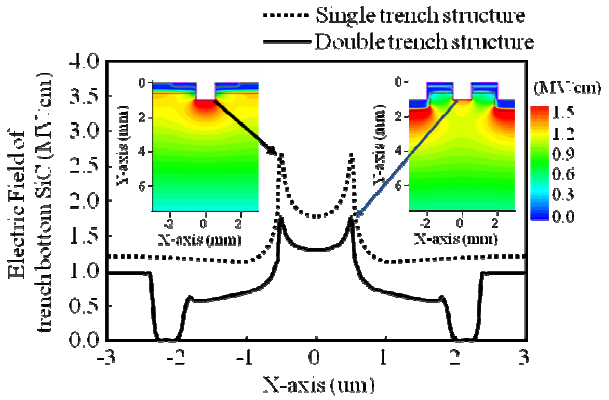

Fig.3 Drain-source bias simulation results at 600V in gate-source voltage 0V.

Fig.4 shows the characteristics of the trench MOSFETs using two different epilayers. The Ron,sp of these was estimated at 0.79 mΩcm^2 (V_B=600V class) and 1.41mΩcm^2 (V_B=1200V class) , respectively. We could achieve ultra low on-resistance while maintaining the high reliability of the gate oxide.

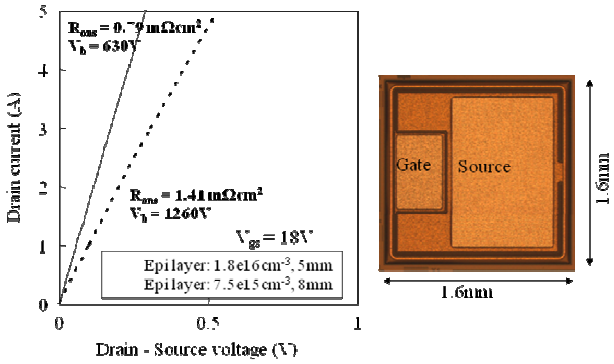

Fig.4 Id – Vds characteristics of double-trench MOSFETs when Vgs = 18 V. The chip size is 1.6 mm x 1.6 mm. Active area is 0.01422 cm^2.

The stability of Vth (Threshold Voltage) during negative gate bias conditions is also an important issue for SiC MOSFETs. Fig.14 shows the time dependence of Vth with a constant negative gate bias of Vgs = -18 V at 150 ^{o}C. The number of test devices was 22. Vth was considerably stable and the change rate was less than 5% after 3000 hours.

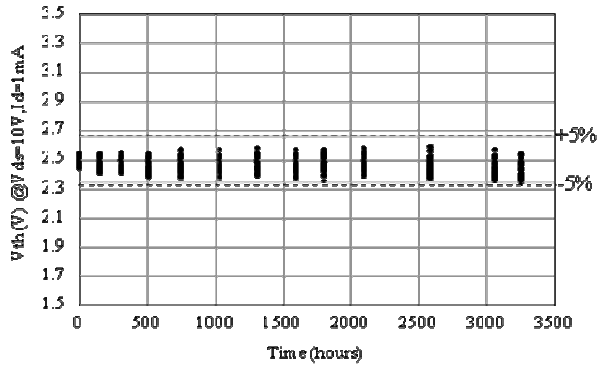

Fig.5 The time dependence of Vth in the constant negative gate bias of Vgs = -18 V at 150 ^{o}C. The number of test device was 22 pcs. Device size was 1.2 x 2.4 mm^2.

3. Conclusions

The two devices presented in this paper, SiC Trench Structure Diode and MOSFET, demonstrate significant performance improvements over conventional devices. In the case of the diode, the incorporation of a trench structure allows a reduction in leakage current with a minimal increase in on-resistance. This is accomplished by reducing the electric field at the Schottky interface without altering the drift layer by extending trenches into the p-type region where high electric fields are experienced. The double-trench MOSFET fabricated, with its lack of a JFET region, achieves class-leading low on-state resistance. By utilizing this trench structure, problems associated with oxide destruction were eliminated by reducing the electric field at the gate bottom.

Acknowledgements

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References

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