# Characterization of gate-control efficiency in AlN/AlGaN/GaN metal-insulatorsemiconductor structure by capacitance-frequency-temperature mapping

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## 1 Introduction

AlGaN/GaN metal-insulator-semiconductor heterojunction field-effect transistors (MIS-HFETs) have attracted much attention. In particular, high-dielectricconstant (high-k) oxide materials, such as  $Al_2O_3$  [1] or  $HfO_2$  [2, 3], have been investigated as a gate insulator of the MIS-HFETs. On the other hand, AlN is an important high-k non-oxide insulator. In addition to AlN-passivated AlGaN/GaN HFETs exhibiting good heat release properties [4–6] due to the high thermal conductivity of AlN ( $\sim 10$  times higher than that of Al<sub>2</sub>O<sub>3</sub>), AlN/AlGaN/GaN MIS-HFETs, where the AlN gate insulator was sputtering-deposited, have been investigated [4, 7, 8], owing to a possible high breakdown field  $\gtrsim 10$  MV/cm and a high dielectric constant  $\sim 10$  comparable to those of Al<sub>2</sub>O<sub>3</sub>. In particular, we showed significant suppression of gate leakage current, although frequency dispersion in the C-V characteristics for forward biases was observed [8]. This dispersion is attributed to the high-density AlN/AlGaN interface mid-gap states leading to poor gate-control efficiency. In this work, for AlN/AlGaN/GaN MIS-HFETs, where the AlN gate insulator was sputtering-deposited, we characterized the gate-control efficiency by capacitancefrequency-temperature (C-f-T) mapping.

#### 2 Experiment and Result

We fabricated AlN/AlGaN/GaN MIS-HFETs and MIS structures simultaneously using an  $Al_{0.29}Ga_{0.71}N$ (25 nm) / GaN (3000 nm) heterostructure obtained by metal-organic vapor phase epitaxy on sapphire(0001). Hall measurements of the heterostructure show an asgrown electron mobility of 1200  $\rm cm^2/V$ -s and a sheet electron concentration of  $1.3 \times 10^{13}$  cm<sup>-2</sup>. On the heterostructure, the Ti/Al Ohmic electrodes were formed and the device isolation was achieved by  $B^+$  implantation. Before AlN gate insulator deposition, we employed two types of surface pretreatments for AlGaN. The first one is organic contaminant removal followed by oxide removal, and the second one is only the organic contaminant removal without the oxide removal. The organic contaminant removal is achieved by organic solvents and oxygen plasma ashing. For the oxide removal, Semicoclean (ammonium-based etchant) is used. After the pretreatments, the AlN gate insulator of  $\sim 19$  nm thickness was deposited on AlGaN surfaces by RF magnetron sputtering at room temperature with an AlN target in Ar-N<sub>2</sub> ambient. The formation of Ni/Au gate electrode completed the device fabrication. As shown in Fig. 1, the MIS-HFETs (left) have the gate length of

250 nm, the source-gate spacing of 2  $\mu$ m, the gate-drain spacing of 3  $\mu$ m, and the gate width of 50  $\mu$ m, while the MIS structures (right) have the 100  $\mu$ m × 100  $\mu$ m area gate electrode surrounded by the grounded Ohmic electrode.

In Fig. 2, we show transfer characteristics of the fabricated MIS-HFETs obtained by the first type surface pretreatment (with oxide removal) and the second one (without oxide removal). Owing to good insulating properties of the AlN, gate leakage currents are significantly small,  $10^{-9}$  A/mm range or less, for both reverse and forward biases. However, we observe a rapid decrease in the transconductance towards forward biases, suggesting poor AlN/AlGaN interface conditions.

In order to investigate the AlN/AlGaN interface properties, we measured the capacitance-voltagefrequency (C-V-f) characteristics of the MIS structures at temperatures from 150 K to 393 K. Figure 3 shows C-V-f characteristics at 150 K and 393 K. We observe frequency dispersion at forward biases for both devices at 393 K. However, the device with oxide removal exhibits a smaller dispersion, suggesting the improved AlN/AlGaN interface. From the measurement results, we obtained the C-f-T mappings, as shown in Fig. 4 at gate voltages 3 V and 0 V with contours. The contours exhibit a straight line behavior, which can be explained by the equivalent circuit of the MIS structures. The equivalent circuit consists of a semiconductor capacitance  $C_{\rm s}$ , an interface state capacitance  $C_{\rm i}$ , and an interface state conductance  $G_i$  in parallel, with an insulator capacitance  $C_0$  connected in series, giving a total admittance

$$Y = \frac{1}{Z} = \left(\frac{1}{jC_{\rm o}\omega} + \frac{1}{G_{\rm i} + jC_{\rm s}\omega + jC_{\rm i}\omega}\right)^{-1} \quad (1)$$

with  $\omega = 2\pi f$ . Since  $C_i$  and  $G_i/\omega$  are functions of only  $\omega \tau$ , where  $\tau$  is the electron trapping time, the measured capacitance  $C = \text{Im}Y/\omega$  is a function of only  $\omega \tau$ . As a result, the contours in C-f-T mappings are given by  $f \propto 1/\tau \propto \exp(-\beta E_a)$ , from which the activation energy  $E_a$  corresponding to the interface state level can be extracted. Figure 5 shows gate voltage dependences of  $E_a$  for the devices with and without oxide removal, obtained by the contours in the C-f-T mappings, with the inset illustrating the band bending and  $E_a$ . Since an effective modulation of  $E_a$  implies an efficient gate control, we conclude that a better gate-control efficiency is obtained in the case of the oxide removal.

## 3 Conclusion

We characterized the gate-control efficiency of the AlN/AlGaN/GaN MIS structures by C-f-T mapping. As a result, it is clearly shown that the oxide removal treatment is effective for improvements of the gate-control efficiency. This characterization method is useful for investigation of gate-control efficiency in the MIS structures.

## References

- T. Hashizume, S. Ootomo, and H. Hasegawa, Appl. Phys. Lett. 83, 2952 (2003).
- [2] C. Liu, E. F. Chor, and L. S. Tan, Appl. Phys. Lett. 88, 173504 (2006).
- [3] A. Kawano, S. Kishimoto, Y. Ohno, K. Maezawa, T. Mizutani, H. Ueno, T. Ueda, and T. Tanaka, Phys. Status Solidi C 4, 2700 (2007).
- [4] Y. Liu, J. A. Bardwell, S. P. McAlister, S. Rolfe, H. Tang, and J. B. Webb, Phys. Status Solidi C 0, 69 (2002).
- [5] N. Tanaka, Y. Sumida, H. Kawai, and T. Suzuki, Jpn. J. Appl. Phys. 48, 04C099 (2009).
- [6] N. Tsurumi, H. Ueno, T. Murata, H. Ishida, Y. Uemoto, T. Ueda, K. Inoue, and T. Tanaka, IEEE Trans. Electron Devices 57, 980 (2010).
- [7] R. Stoklas, D. Gregušová, Š. Gaži, J. Novák, and P. Kordoš, J. Vac. Sci. Technol. B 29, 01A809 (2011).
- [8] H.-A. Shih, M. Kudo, M. Akabori, and T. Suzuki, Jpn. J. Appl. Phys. 51, 02BF01 (2012).

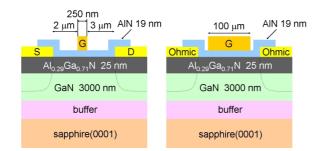


Fig. 1: Schematic cross sections of the fabricated MIS-HFET (left) and MIS structure (right).

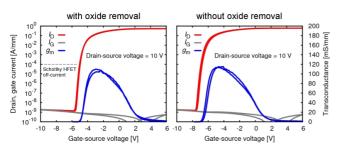


Fig. 2: Transfer characteristics of the MIS-HFETs. Drain current  $I_{\rm D}$ , gate current  $I_{\rm G}$ , and transconductance  $g_{\rm m}$  were obtained under the gate voltage sweep of  $-10 \text{ V} \rightarrow +6 \text{ V} \rightarrow -10 \text{ V}$ .

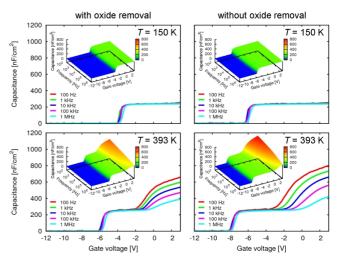


Fig. 3: C-V-f characteristics at 150 K and 393 K of the MIS structures.

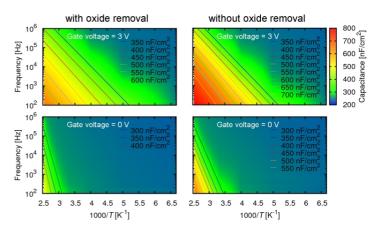


Fig. 4: The C-f-T mappings of the MIS structures for the gate voltages 3 V and 0 V with contours.

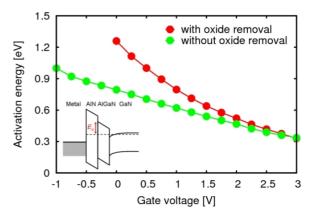


Fig. 5: The gate voltage dependence of activation energy obtained by contours in C-f-T mappings.