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Fully Transparent AZO Thin-film Transistors Fabricated on Flexible Plastic Substrates at Room Temperature

Wei Wang[1], Dedong Han[1]*, Jian Cai[1], Youfeng Geng[1], Liangliang Wang[1], Yu Tian[1], Yi Wang[1] and Shengdong Zhang[2]*

[1]Institute of Microelectronics, Peking University, Beijing 100871, PRC
[2]Shenzhen Graduate School, Peking University, Shenzhen 518055, PRC
Phone: +86-10-6275-3144 Fax : +86-10-6275-1789 *E-mail: handedong@pku.edu.cn, zsd@ime.pku.edu.cn

1. Introduction

Flexible transparent electronics based on thin-film transistors (TFTs) has been regarded as an important role in next generation display technology because of its advantages such as being conformable, thin profile and light weight [1]. The main challenge of flexible thin-film transistors is to find appropriate channel materials and improve fabrication methods to get over the inherent barrier of the low glass transition temperature (*Tg*) for flexible substrates [2]. There has been extensive interest in examining transparent oxide semiconductors as the channel material of TFTs due to their superior optical and electrical properties in spite of low-temperature process [3-5]. One effective method to improve the device performance without increasing the process temperature is to adopt the composite channel structure and combine films with desirable features [6-8]. In this paper, we fabricate TFTs using Al-doped ZnO (AZO) as channel materials on flexible plastic substrates at room temperature and further investigate the structure of dual channels composed a high-density layer and a low-density layer.

2. Experiments

The carrier concentration of the AZO film is mostly related to the oxygen vacancies in the film. Thus we changed the carrier concentration in the film through controlling the oxygen content in deposition feed gas during the rf magnetron sputtering and prepared the dual channels composed a high-density layer and a low-density layer.

In this fabrication, the conventional bottom-gate structure and the 3-mask lithography and lift-off process were adopted. The structure schematic is shown in Fig. 1. A kind of transparent PET plastic was used as the substrate.

First, a 120nm-thick ITO layer was sputtered on the PET substrate and then lift-off to form gate electrodes. Afterwards, a gate insulator of 150nm SiO_2 was deposited by PECVD. Then the dual channels were formed by successive deposition of a 15nm AZO layer and then a 75 nm AZO layer, of which the O_2/Ar ratio during the rf magnetron sputtering was 0/100 and 5/95 respectively. The three layers were lift-off together to form the gate insulator and the channel. Lastly a 200nm ITO layer was sputtered as the source and drain contacts. The whole fabrication was carried out at room temperature and no intentional heating was performed during the deposition step. We also fabricated TFTs with the single AZO channel deposited under the O_2/Ar ratio of 5/95 for comparison. Thin-film transistors as-fabricated were fully transparent-looking (seen in Fig.2), with W/L= 10 and L = 10μm.

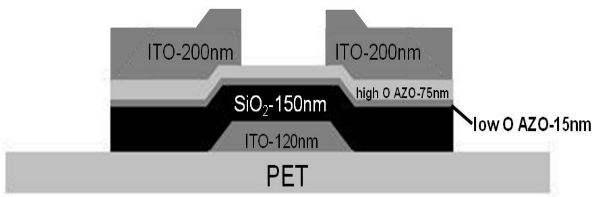

Fig. 1 Schematic of a dual-channel AZO thin- film transistor on PET substrate

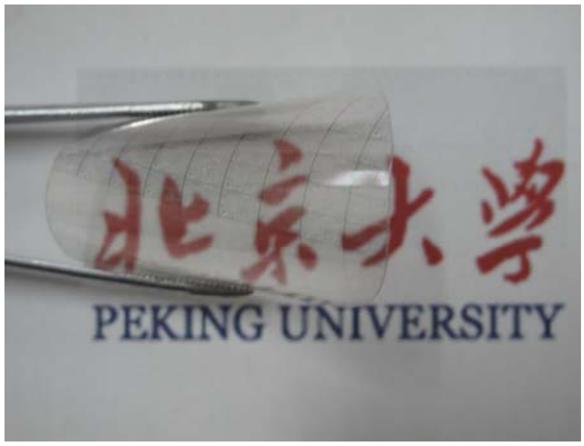

Fig. 2 Image of transparent AZO thin- film transistor on a bent flexible PET substrate

3. Results and discussion

The transfer characteristics of AZO TFTs with two kinds of channel structures are illustrated in Fig. 3, analyzed by a semiconductor parametric analyzer (Agilent 4156C). The drain voltage (V_D) was set at 5V, while the gate voltage (V_G) ranged from -5~15V. Table Ⅰ shows the extracted electrical parameters of AZO TFTs with two kinds of channel structures.

As can be seen from the table, by changing from a single to a dual-channel structure, the saturation mobility was increased by an order of magnitude, from 3.13 to

$31.4 cm^2V^{-1}s^{-1}$, while the threshold voltage (V_{th}) was 3.85V, almost unchanged. The Subthreshold Swing (SS) decreased and was 0.33V/dec. The drain current on/off ratio was also enhanced by about an order of magnitude and reached up to about 10^8.

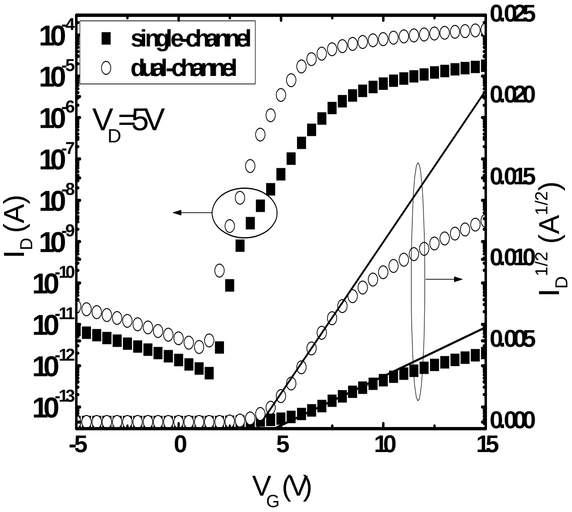

Fig. 3 Representative transfer characteristics of AZO TFTs with two kinds of channel structures.

Table I The extracted electrical parameters of AZO TFTs with different channel structures

Channel structure	V_{th} (V)	SS (V/dec)	μ_{sat} $(cm^2V^{-1}s^{-1})$	I_{on}/I_{off}
Single-channel	4.82	0.46	3.13	$\sim 10^7$
Dual-channel	3.85	0.33	31.4	$\sim 10^8$

Fig. 4 shows the SEM image of two kinds of AZO films. It can be seen obviously that with the O_2/Ar ratio increasing during the deposition, the grain size of AZO films decreases, which means better uniformity in film properties.

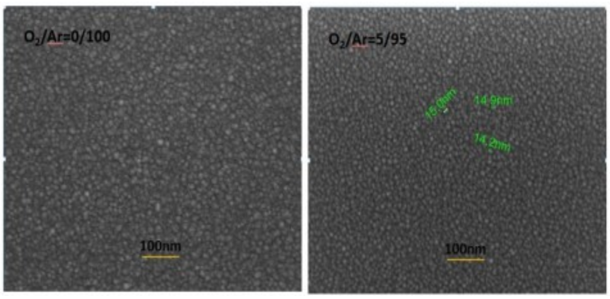

Fig. 4 SEM image of the AZO films. The grain size decreases with the increasing O_2 partial pressure.

This double-stacked channel structure provides a possibility to improve the mobility, the on-current and meanwhile restrain the off-current. It's just the combination of these two layers with their respective desirable features that causes this device improvement. The carrier mobility depends exponentially on the grain size because of the grain boundary scattering, which is dominant over the ionized impurity scattering in AZO films [9]. Therefore we actually got an AZO layer of high carrier density as well as high carrier mobility close to the gate insulator, which precisely forms the carrier generation layer in thin-film transistors [10]. On the other hand, the thick AZO layer close to the source and drain contacts forms the main transport channel through which the electrons flow from the source to the drain. Therefore it can help to restrain the source-to-drain leakage current when the device is turned off due to its low carrier concentration. Besides, the good uniformity can help to ensure the device a stable electrical performance such as a suitable V_{th}.

4. Conclusions

A double-stacked channel structure has been developed to improve the electrical performance of transparent flexible thin-film transistors using Al-doped ZnO as channel materials. Compared with the single-layer device, the saturation mobility is increased by an order of magnitude and reaches $31.4 cm^2V^{-1}s^{-1}$, while the threshold voltage is 3.85V, almost unchanged. The subthreshold swing decreases and is 0.33V/dec. The drain current on/off ratio is also enhanced by about an order of magnitude and reaches up to about 10^8. This improvement is achieved by combining a high-density layer and a low-density layer as the active layer. Besides, it doesn't require a high-temperature annealing and is compatible with the process of thin-film transistors on flexible substrates.

Acknowledgements

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References

[1] L. Zhou and A.Wanga, *Appl. Phys. Lett.*(2006) 083 502.

[2] Nai-Chao Su, Shui-Jinn Wang, *Electron Device Letters* (2010) 680.

[3] T. Kamiya, K. Nomura, and H. Hosono, *Sci. Technol. Adv. Mater.* (2010) 044 305.

[4] S. Yang, D.-H., Cho, *Appl. Phys. Lett.* (2010) 213 511.

[5] E. Fortunato, L. Pereira, *Appl. Phys. Lett.* (2008) 222 103.

[6] Michael A. Marrs and Curtis D. Moyer, *Transactions on Electron Devices* (2011) 3428-3434.

[7] Jae Chul Park and Ho-Nyeon Lee, *Electron Device Letters* (2012) 0741-3106.

[8] S. I. Kim, C. J. Kim, J. C. Park, *IEDM Tech. Dig.* (2008) 7376

[9] Kun Ho Kim, *J. Appl. Phys.* (1997) 7771.

[10] A. C. Tickle, *Thin-Film Transistors: A New Approach toMicroelectronics*. Hoboken, NJ: Wiley, (1969).