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High-Performance Transparent Top-Gate AZO TFTs Fabricated by Low-Temperature Process

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1. Introduction

Oxide semiconductor thin film transistors (TFTs) have drawn increasing attention for their excellent optical and electrical properties in driving active matrix OLED and other displays[1~5]. In particular, Zinc Oxide based TFTs have received the most considerable attention, especially a-IGZO TFTs. However, In element is a toxicant, rare one on earth and going to be exhausted, so a non-In active channel layer offers competitive advantages, such as lower cost, higher throughout, and safety. In this experiment, we choose Al-doped ZnO (AZO) as active channel layer as Al is abundant in earth, harmless to human beings and, thereby, very low manufacturing cost. Some articles about AZO TFTs have been reported in the literature, however, the device performance presented was not very good[3]. In this letter, we successfully demonstrate fully transparent top gate type AZO TFTs on glass substrates by a simple process using only two photomasks. All the process temperature was below 100℃. The effects of O_2 incorporation during the formation of the active layer were analyzed by comparing the characteristics of devices with and without oxygen incorporation. The performance of the device was improved greatly due to the O_2 incorporation. As for TFTs we demonstrated devices with subthreshold swing of 125 mV/decade, saturation mobility of 113 $cm^2/V\bullet s$, threshold voltage of 1.5V, I_{off} value of 10^{-13}A, on/off ratio of 1×10^9 for V_G = -2 to 5V operation, high transmittance of 82.5%, which, to our knowledge, are among the best ever reported.

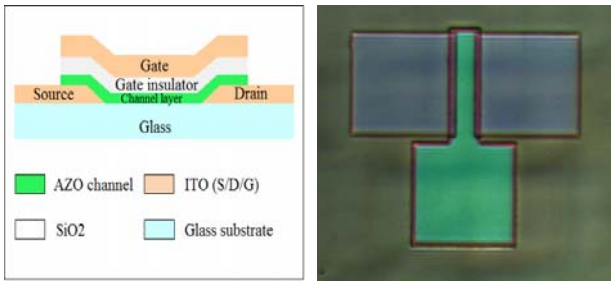
2. Device Fabrication

In this experiment, the growth chamber was first pre-pumped to the base vacuum pressure of 5×10^{-4} Pa. The total working pressure was of 1 Pa. No intentional substrate heating was performed during each deposition step. The cross-section view of the inverted staggered top gate architectures is shown in Fig. 1(a), and the top view of the AZO TFT (W/L=50 μ m/10 μ m) is shown in Fig. 1(b).

The fabrication procedure for the AZO TFT was as follows: First, a 150 nm thick ITO film was deposited at room temperature by RF sputtering in pure Ar atmosphere using a target of ITO and patterned to form the S/D electrodes. Then, a stack of 100 nm thick channel layer (AZO), 150 nm thick gate insulator (SiO_2) and 150 nm thick gate electrode (ITO) was deposited sequentially: the active channel and the gate electrode were sputter deposited at room temperature; the gate insulator was deposited by PECVD at 80℃. Finally, the stack of the active channel, gate insulator and gate electrode was patterned to form the channel, gate insulator and gate electrode, respectively.

To investigate the effects of the O_2 incorporation during the formation of active channel layer, we designed two different kinds of TFTs, named U1 and U2. As for U1, the channel was deposited in pure Ar atmosphere, while for U2 in a mixed atmosphere of Ar and O_2, the O_2 flow ratio was 3%.

Surface morphology of the AZO films were evaluated by atomic force microscopy (AFM). The TFTs were electrically characterized at room temperature by a semiconductor parameter analyzer (Agilent 4156C).



(a) (b)

Fig. 1 (a) Schematic cross section of the top gate type AZO TFT (b) The top-view of a fabricated AZO TFT (W/L=50 μ m / 10 μ m).

3. Analysis and Discussion

Fig. 2 shows the transfer characteristics of the U1 and U2 TFTs (W/L=50 μ m/10 μ m) as fabricated without any post annealing process. The off-state current of U1 is very high, however, due to the incorporation of O_2 in the deposition of the channel layer, the U2 exhibits a much lower off-state current of 10^{-13} A while maintaining a relatively high on-state current. For the transfer characteristic at V_D=5V, the U2 device demonstrates excellent properties, such as a much higher on/off ratio of 1×10^9, a much steeper subthreshold slope of 125 mV/decade, a threshold of 1.5 V, a saturation mobility μ_{sat} of 113 $cm^2/V\cdot s$. The threshold voltage (V_{th}) and the saturation mobility (μ_{sat}) were extracted from the saturation regime when V_D=5V, which was

higher than most recent reports on ZnO-based TFTs[3-5]; the subthreshold slope (S) was extracted from the curves of $dV_G/dlog_{10}I_D$ versus V_G in the saturation regime, and the smallest value was taken. The inset picture shows the output characteristic of the U2 TFT, which is well-behaved, exhibiting an apparent pinch off and drain current saturation at sufficiently high drain biases. Table I compares the important device parameters of the AZO TFT with those on glass substrates reported in the literature. The high mobility, steep subthreshold slope and high on/off ratio in the present work are among the best ever reported.

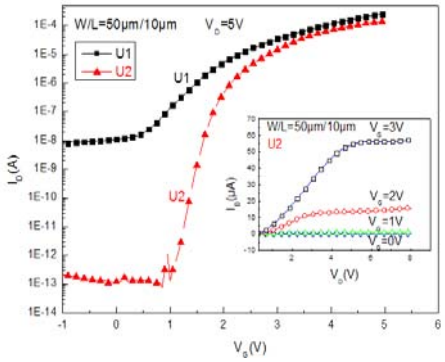
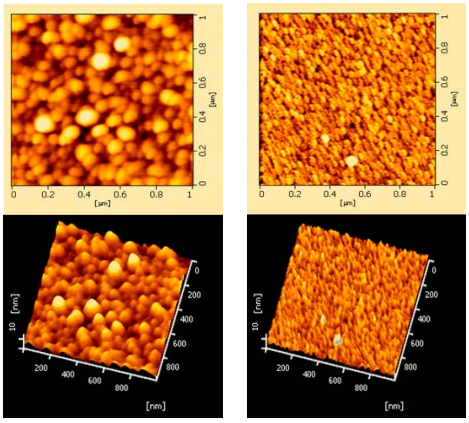


Fig. 2 The transfer curves of the U1 and U2 TFTs. The output characteristic of the U2 TFT is shown in the inset picture.

Table I Comparison of TFTs Fabricated on Glass Substrates

No.	Structure type	Channel Material	Max Process Temp (℃)	μ_{sat} (cm^2/V•s)	S(V/decade)	On/off ratio
This work	Top	AZO	100	113	0.125	1×10^9
[3]	Bottom	AZO	300	1.66	2.7	5×10^2
[4]	Top	ZnO	-----	40.5	0.23	1.2×10^7
[5]	Top	IGZO	200	24.7	0.203	1×10^8

Fig. 3(a) shows the AFM surface morphology of the AZO films of U1. Fig. 3(b) shows that of U2. From the AFM images in Fig. 3, the AZO films of U1 and U2 exhibit a granular surface morphology with an RMS surface roughness of 1.801 nm and 1.222 nm, respectively. The U2 get a much smaller RMS value, which indicates a more smoothing surface as is manifest in Fig. 3. We have measured the transmittance of the AZO films of U1 and U2, and the transmittance of the TFTs of U1 and U2, as is shown in Fig. 4. We find that the average transmittance of the AZO film of U2 in the infrared range and near UV range is higher than that of U1, and that the average transmittance of the TFTs of U2 is of 82.5% in the whole range, which is higher than that of U1. It can be concluded that during the RF sputtering deposition of AZO active channel film, the incorporation of O_2 in the atmosphere can effectively improve both the surface morphology and the transmittance qualities of the AZO film.



(a) (b)

Fig. 3 The AFM images of the AZO channels' surface topographies (a) of U1, and (b) of U2.The scan size is 1μm×1μm.

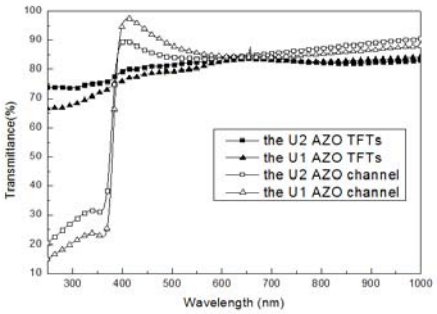


Fig. 4 Transmittance of the AZO films and the AZO TFTs as fabricated on glass.

4. Conclusions

In conclusion, we have successfully fabricated a staggered top gate type AZO TFT on glass substrate by a simple process. All the process is done under 100℃, which can be well applied on flexible substrate. The AZO TFT with O_2 incorporation during the deposition of channel layer shows excellent properties. This device is suitable for active devices in large area and low cost display applications.

Acknowledgments

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