Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials, Kyoto, 2012, pp917-918

Reverse Gate Bias Stress on high-voltage AlGaN/GaN-on-Si Heterostructure FETs

Shinhyuk Choi[1], Jae-Gil Lee[1], Hoonsang Yoon[1], Ho-Young Cha[1], and Hyungtak Kim[1]

[1] School of Electrical Engineering
Hongik University, Seoul 121-791, Korea, Republic of.
Phone: +82-2-320-3013 E-mail: shinhyuk001@hanmail.net

1. Introduction

GaN technology is the most promising candidate for power switching applications which require high breakdown voltage and low on-resistance. To compete against Si-based power devices, GaN-on-Si technology is inevitable for low total fabrication cost.

A GaN-based transistor has been developed and is being commercialized in the area of high frequency applications. Before its commercialization, the degradation mechanisms had to be elucidated to improve reliability and several groups have made tremendous efforts to figure out these phenomenon. [1], [2] However, reliability study on high-voltage GaN-on-Si devices designed for high power switching application has seldom been reported.

In this work, DC bias stress tests have been performed on high voltage AlGaN/GaN Heterostructure FETs(HFETs) on Si substrate. The devices were submitted to reverse gate bias stress tests to determine the dominant degradation mechanism. The stressed devices showed a particular point of a sharp increase of gate leakage current and these devices were degraded permanently in terms of gate leakage. Both the gate edge of source and drain side were damaged even if either source or drain was floated under different stress conditions. In addition, the time dependent degradation was observed by a constant gate bias stress test.

2. Device Fabrication

A cross sectional view of AlGaN/GaN HFETs used for this work was shown in Figure 1. The devices were fabricated on epitaxial structures which consist of a 4-nm undoped-GaN capping layer, a 20-nm undoped-$Al_{0.23}Ga_{0.77}N$ barrier, a 1-nm AlN spacer, a 1.7-μm undoped-GaN buffer, and an undoped AlN/AlGaN/GaN transition layers grown on an N-type Si(111) substrate. [3] The tested devices have a gate length of 2-μm, a gate-source and a gate-drain distance of 3-μm and 15-μm, and a gate width of 100-μm, respectively. Ti/Ni/Ir/Au (1-nm / 20-nm / 20-nm / 360nm) metals form Schottky gates and gate field plates which have various lengths of 1-μm, 2-μm, 8-μm, and 10-μm, respectively. A Si/Ti/Al/Mo/Au (5-nm / 20-nm / 60-nm / 35-nm / 50-nm) layer was evaporated and annealed in a N_2 ambient at 830℃ for 30 sec for source and drain ohmic contacts. The devices were passivated with SiN_x layer (~500-nm).

3. Stress Experiments

We used a step-stress method (ΔV_G = -1 V, from -10 V to -50 V, 1 minute for each step) for these devices which demonstrated high breakdown voltage of 816 V, 750 V, 742 V, and 615 V with respect to the gate field plate lengths. [1] The devices with 1-μm field plate were step-stressed by a reverse gate bias under two different bias conditions including V_D=0 V with source floated and V_{DS}=0 V and the result is shown in Figure 2. The electric field which can induce the inverse piezoelectric effect between gate and either drain or source strengthens as increasing gate voltage, then a sudden increase of reverse gate current was observed when it reached a particular value which is named critical voltage (V_{CRIT}). [1], [4] Under D-G stress (V_D=0 V), the electric field between gate and source is weaker than V_{DS}=0 V stress due to device asymmetry, and induced the higher V_{CRIT}.

Next, we investigated which side of gate edge was degraded during stress tests. Two-terminal stress test, V_{SG} and V_{DG} stress were performed, and then reverse gate current of drain-gate (DG) diode and source-gate (SG) diode were measured. At the beginning of this work, we had expected that SG diode was only damaged under V_{SG} stress, however increase of DG diode reverse gate current was also observed (Figure 3(c)) from the result. The same phenomenon was also found under V_{DG} stress (Figure 3(b)). This experimental result suggests that both edges of gate were affected by the stress irrespective of location of defects created by inverse piezoelectric effect.

We also observed the time dependent degradation using a constant gate bias stress test. [5] Before the test, the device was step-stressed under V_{DS} =0 V and V_{CRIT} was observed at -30 V of V_G. Thus, the device was stressed with -25V gate voltage. Even though the gate voltage was less than V_{CRIT} sudden increase of reverse gate current was observed after 2100s (Figure 4(a)) and the reverse gate current of both DG and SG diodes were increased permanently (Figure 4(b)). This is the experimental evidence that there is a correlation between time and the degradation characteristics.

Through these whole experiments, we have not seen any significant changes of on-current not only under the step-stress (Figure 5(a)), but also under the constant bias stress (Figure 5(b)) while we observed increase of reverse gate current. It means that the inverse piezoelectric effect is broken out earlier than the hot carrier injection. [6]

4. Conclusions

We investigated the degradation characteristics of high BV AlGaN/GaN HFETs-on-Si with various stress condi-

tions. We observed V_{CRIT} which was occurred by the inverse piezoelectric effect under V_{DS} and V_{DG} stress tests and dependence of electric field strength. with V_{DG} and V_{SG} stress tests, we obtained the experimental evidence that the gate edges of both source and drain side were damaged regardless of occurrence place of inverse piezoelectric effect. The degradation mechanism has a time dependent element and the constant bias stress experiment underpinned this argument.

Acknowledgements

This research was supported by the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2012-0003993).

References

[1] J.A. del Alamo and J. Joh, *Microelectron. Reliab.,* vol. 49, nos. 9-11, pp. 1200-1206, September –November 2009.

[2] G. Meneghesso, G. Verzellesi, F. Danesin, F. Rampazzo, F. Zanon, A. Tazzoli, M. Meneghini, and E. Zanoni, *IEEE Trans. Device Mater. Rel.,* vol. 8, no. 2, pp. 332–343, Jun. 2008.

[3] Jae-Gil Lee, Ho-Jung Lee, Ho-Young Cha, Minseong lee, Yeonmi Ryoo, Kwang-Seok Seo, and Jea-Kyoung Mun, *J Kor. Phys. Society*, vol. 59, no. 3, pp. 2297-2300, September 2011.

[4] S.Y. Park, C. Floresca, U. Chowdhury, J. L. Jimenez, C. Lee, E. Beam, P. Saunier, T. Balistreri, and Moon J. Kim, *Microelectron. Reliab.,* vol. 49, pp. 478-83, 2009.

[5] M. Meneghini, A. Stocco, M. Bertin, D. Marcon, A. Chini, G. Meneghesso, and E. Zanoni, *Appl. Phys. Lett.,* vol. 100, no. 3, pp. 033505-1–033505-3, Apr. 2012.

[6] H. Kim, R. M. Thompson, V. Tilak, T. R. Prunty, J. R. Shealy, and L. F. Eastman, *IEEE Electron Device Lett.*, vol. 24, no. 7, pp. 421–423, Jul. 2003.

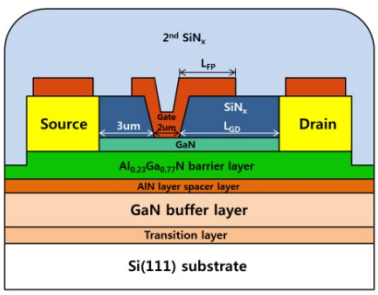

Fig. 1 A cross sectional view of AlGaN/GaN HFETs-on-Si.

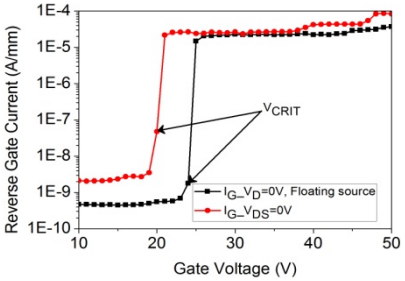

Fig. 2 The step reverse gate bias stress test under V_{DG}(Source-floated) and V_{DS} conditions. V_{CRIT} was observed at -24V (V_{DG}) and -20V (V_{DS}).

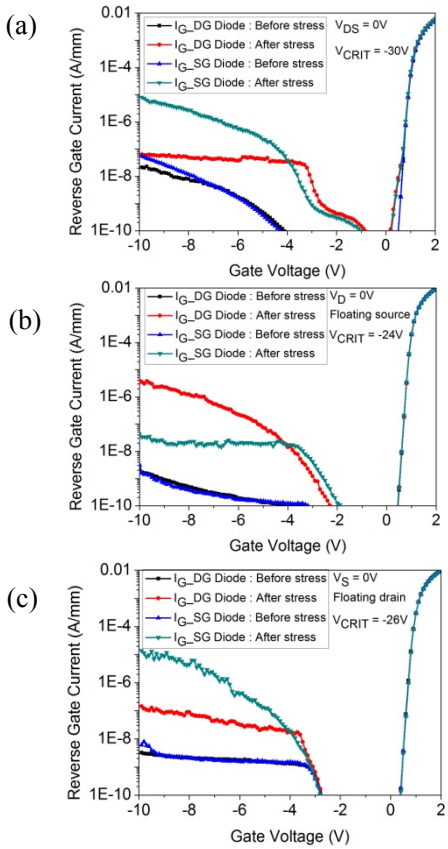

Fig. 3 The reverse gate current of DG and SG diodes under (a) V_{DS}, (b) $V_{DG(source\text{-}floated)}$, and (c) $V_{SG(drain\text{-}floated)}$ conditions. The devices have (a) 8-μm and (b), (c) 10-μm field plate lengths, respectively.

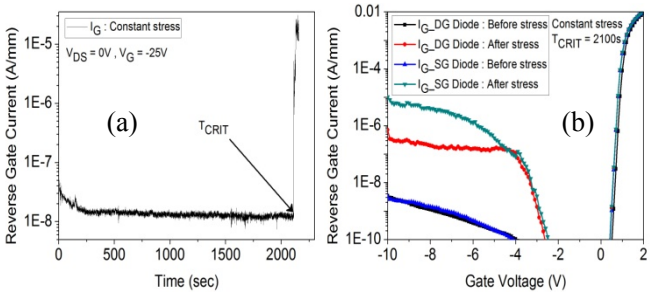

Fig. 4 The constant reverse gate bias stress test under V_{DS} condition. Reverse gate current (a) during the stress and (b) of DG and SG diodes. The devices have 2-μm field plate length.

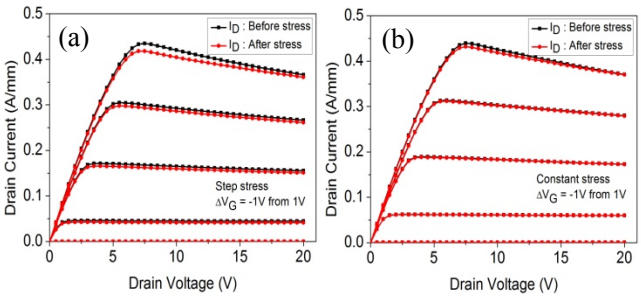

Fig. 5 The I-V characteristics of (a) the step-stress test and (b) constant bias stress test. The devices have 2-μm field plate length.