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Performance Revelation and Optimization of Gold Nanocrystal for Future Nonvolatile Memory Application

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1. Introduction

Recently, nanocrystal (NC) memory has been widely investigated due to the potential advantages for the prevention of higher leakage current caused by thinner tunneling layer [1].Among all the NC materials, gold (Au) is one of the most valuable candidates because of its high work function and simple rapid thermal annealing (RTA) formation process [2]. The uniform Au NCs via RTA process can be formed because of the condensation effect during the rapid thermal heating and cooling procedure [2-3]. However, the annealing temperature effects on the electrical characteristic still remain unknown. In this paper, the annealing temperature effects on the memory characteristic was revealed and optimized

2. Experiments

First, the n-type Si wafers were cleaned. Second, the thermal oxidation process was conducted to form a 3nm SiO_2. Then, Au thin film ~2nm was deposited by E-beam evaporation and subsequently annealed by RTA system. Four different annealing temperature, 500, 600, 700, and 800^{o}C, were used to form Au NCs. Next, a 10nm SiO_2 as the blocking oxide was deposited via plasma enhanced chemical vapor deposition (PECVD) system. All samples were plated with Al as a gate electrode. The C-V hysteresis was measured by using HP4285 LCR meter and the gate pulse was supplied by using HP8110A. The process flow and device schematic are shown in Fig.1.

3. Results and discussion

Fig.2 shows the SEM planar images of Au NCs. The average Au NCs diameters were 6-8nm which had a less dependence with the annealing temperature, as shown in Fig.3. On the other hand, the Au NCs densities were increased with increasing annealing temperature. This is because of more nucleation sites and higher surface mobility with increasing temperature [3]. The typical C-V hysteresis curves could be observed, as shown in Fig.4. Note that there was no hysteresis phenomenon for the sample without Au NCs, as shown in the inset. Fig.5 shows the program/erase speed of the devices. It was found that the higher program speed was obtained with increasing annealing temperature, while the erase speed had a less dependence with the annealing temperature. The higher program speed is owing to the higher Au NCs density, i.e., more storage nodes for electrons. The retention characteristic at room temperature (25^{o}C) is shown in Fig. 6. The lowest charge loss percentage can be found for 700^{o}C annealing temperature. The inset shows the retention at 25^{o}C, 55^{o}C and 85^{o}C for 700^{o}C sample. To explain the retention degradation for 800^{o}C sample, we evaluated the charge loss activation energy (Ea) related to the retention temperature. The extraction method of activation energy was identical with ref. [4]. Fig.7 shows that the highest activation energy (0.1075eV) was obtained for 700^{o}C sample. In the high-resolution transmission electron microscopy (HRTEM) image of 700^{o}C sample, as shown in Fig.8, it was found that the thickness of tunneling oxide increased slightly because of the re-oxidation during Au NCs formation process. This is the reason that the charge loss percentage decreased for 700^{o}C sample. The lateral electron migration between Au NCs for high density of Au NCs is responsible for the high activation energy of 700^{o}C sample, as shown in Fig.9. However, too high annealing temperature (800^{o}C) will cause the Au diffusion into tunneling oxide, resulting in the increasing amount of defects. Therefore, traps assist tunneling (TAT) path via those defects could occur, as shown in Fig.10, and reduce the activation energy. Thus, the 700^{o}C annealing temperature for the formation of Au NCs is considered to be the optimized one. The endurance characteristic of 700^{o}C sample was also conducted, as shown in Fig.11. Though the small V_{FB} shift after 10^4 operation cycles was observed, the memory window still remained ~1V. It is worthy note that the oxide has no degradation after cycling operation, as shown in the inset of Fig.11.

4. Conclusion

This paper reveals that an appropriate Au NC formation annealing temperature is optimized for the future advanced NC memory application. The electrical performance shows the good reliability of this device.

Acknowledgements

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References

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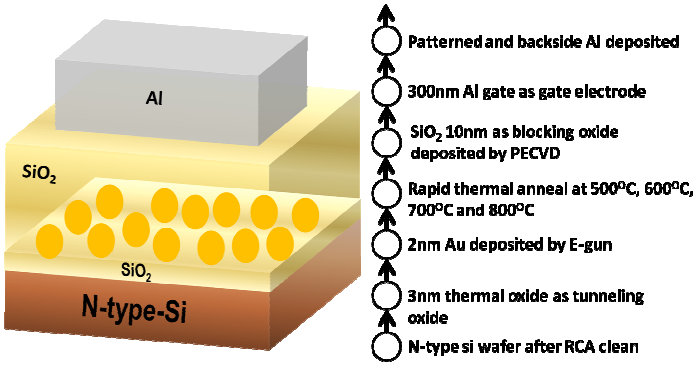

Fig. 1 The schematic of device process flow and structure.

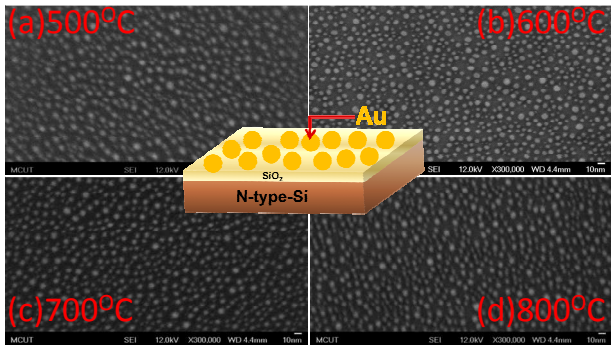

Fig. 2 The planar SEM images for Au nanocrystal of four different annealing temperature.

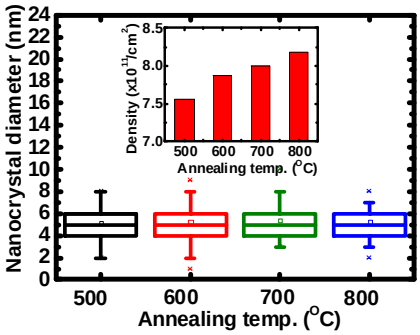

Fig. 3 The Au nanocrystal diameters and densities versus annealing temperature.

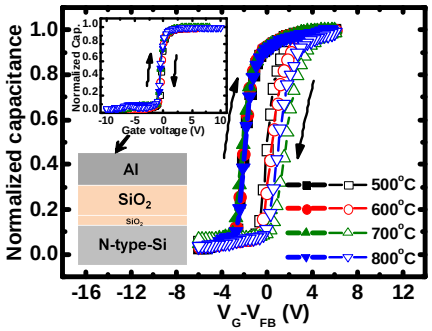

Fig. 4 C-V hysteresis curves of the Au nanocrystal memory. Inset shows the neglected hysteresis of the sample without Au nanocrystal.

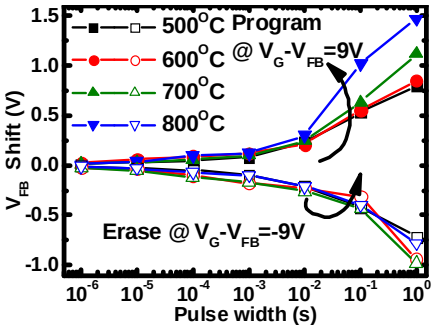

Fig. 5 The program/erase speed of the Au nanocrystal memory. The program and erase condition was V_G-V_{FB} = 9V and -9V, respectively.

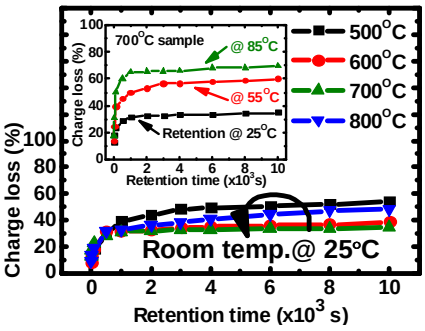

Fig. 6 The retention characteristic of Au nanocrystal memory at 25°C. The inset shows the retention at 25, 55, 85°C for 700°C sample.

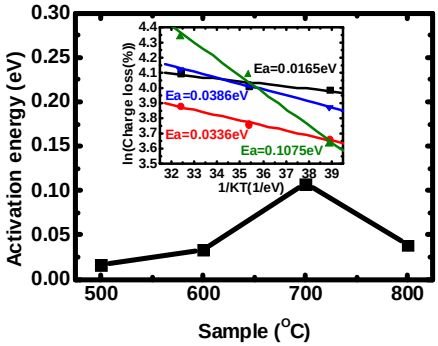

Fig. 7 The activation energy related with the charge loss for Au nanocrystal memory. Inset shows the logarithm of charge loss versus 1/kT.

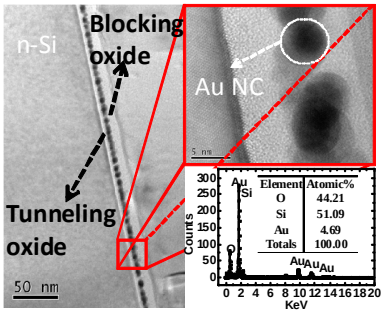

Fig. 8 The cross sectional HRTEM image and O, Si, and Au atomic percentage by EDX analysis of Au nanocrystal memory.

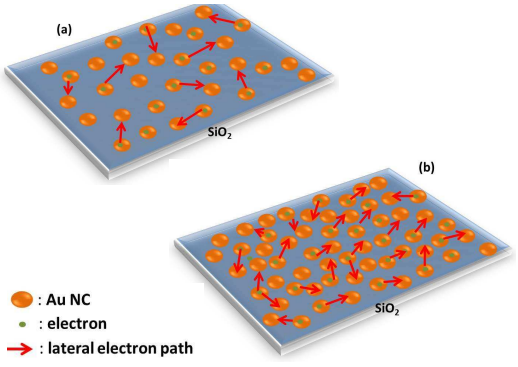

Fig. 9 The schematic of lateral electron migration for (a) low and (b) high Au nanocrystal density.

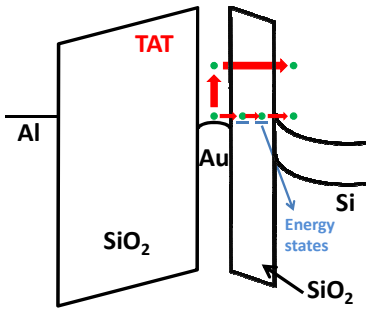

Fig. 10 The band diagram of Au nanocrystal memory for charge loss via traps assist tunneling (TAT) mechanism.

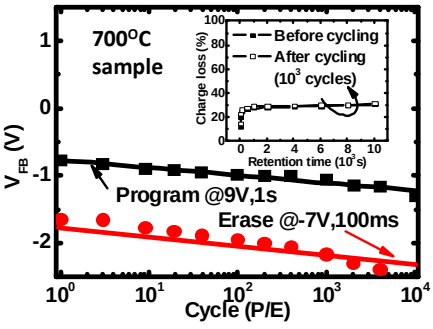

Fig. 11 The endurance characteristic for 700°C sample. Inset shows the retention comparison with fresh sample and the sample after 10^3 cycling operation.