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Placement of Single Ge quantum Dot along with Self-aligned Electrodes for Effective Single Hole Tunneling

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1. Introduction

A SET consists of a nanoscale quantum dot (QD) tunnel coupled to drain and source electrodes, and thus electrons can flow when energy levels of the QD attain resonance with fermi levels of source reservoir under gate and drain modulation, producing characteristic drain current Coulomb oscillations and staircases because of one-particle energy levels and Coulomb interactions. This device offers promising potential for low-power logics [1], memory [2], and of particular quantum information and electrical metrology [3] applications. Over the past decades, elaborate efforts on process evolution have being devoted for the realization of high-performance Si-based SETs [1-7]. For effectively manipulating charges in a SET, it requires not only precise control over the QD shape, size, and crystallinity strongly relating to the QD electronic structure, but also the QD number and location (tunnel junctions) among electrodes. However from a device fabrication perspective, making electrical contacts to a specific nanoscale QD presents an arduous challenge owing to the lithographic limits on the feature size and overlay alignment.

Making use of lithography and selective oxidation of patterned SiGe-on-insulator structures, the authors have demonstrated precise placement and size control of the Ge QD [8, 9], which are separated from electrodes by spacer layers of SiO_2 or Si_3N_4. Importantly tunnel paths between the QD and electrodes are directly determined by the deposited spacer layers whose thickness is easily controlled by deposition techniques in nanoscale. The demonstration of control over the QD placement along with self-aligned electrical contacts may offer a promising solution for coping with the rigorous requirements for SETs.

2. Experimental

In this paper, we advance the aforementioned Ge QD placement technique to realize Ge-QD SHTs with self-aligned electrodes and nanometer-thick tunnel barriers. The schematic diagrams of designed device structure and key process flow are summarized in Fig. 1(a)-(b). Figure 1(c)-(e) shows the scanning electron microscopy (SEM) and transmission electron microscopy (TEM) images of fabricated Ge QD SHTs, in which a single 11 nm Ge QD resides in the center of the trench and self-aligns with NiSi electrodes via a 12-nm-thick tunnel barrier of Si_3N_4. Figure 1(d)–(f) illustrate that after oxidizing a SiGe nanorod bridging a 15-nm-wide trench, a spherical, single crystalline Ge QD is created in the center of the trench and

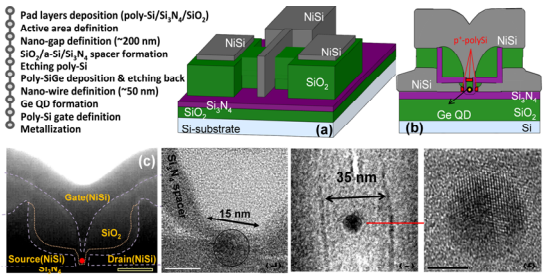

Fig. 1. (a)/(b) schematic device structure of designed SHT, (c)/(d)/(f) cross-sectional and (e) plane-view SEM/TEM images of fabricated Ge QD SHTs.

submerges into underlying pad layer of Si_3N_4. This manifests that proposed QD fabrication technique is able to place a single QD self-aligned with electrodes via tailored tunnel junction, offering a feasible approach for fabricating SETs for analytically resolving the tunneling spectroscopy.

3. Results and Discussion

Ge QDs would be more attractive for use in quantum-tunneling devices because of the higher dielectric constant and lower carrier effective mass of Ge, leading to a large exciton Bohr radius (24 nm for Ge versus 5 nm for Si), below which quantum confinement effects (QCEs) inducing modifications on the electronic structure become significant. As a consequence, the QD size criterion for a SET is reasonably less stringent in the Ge QD than for the Si QD. Charge tunneling through discrete energy levels of the Ge QD appears to be well directed by applied gate (V_G) and drain voltages (V_D). As seen in Fig. 2, there appear distinct I_D plateaus and G_D peaks ($G_D \equiv \partial I_D/\partial V_D$) once V_D

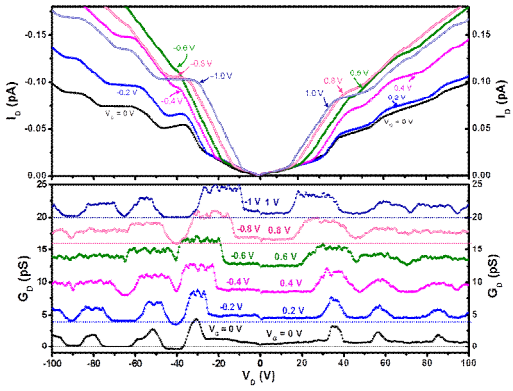

Figure 2 Gate modulated (a) I_D–V_D and (b) G_D-V_D characteristics of Ge QD SHT at T = 120 K. Each G_D curve is vertically shifted by 4 pS for clarity, and the dashed line for each V_G case corresponds to the condition of G_D = 0.

exceeds a threshold value, and the corresponding Coulomb gap declines from 67 to 35 mV with an increase in V_G from 0 to 1V. The polarity-independent threshold voltages for the line-up of ground state (E_1) of the QD with Fermi energies of electrodes evidence the effectiveness of this proposed QD placement technique that produces symmetrical tunnel paths for charges through the QD. A Coulomb gap of 67 mV corresponds to an effective capacitance (C_d + C_s) of 2.39 aF between electrodes, and the estimated QD diameter of 8 nm is slightly smaller than the statistic value (~11 nm) obtained from TEM observations of more than 10 QDs. The QD size is about one-third of the exciton Bohr radius for Ge, leading to strong QCEs wherein. The wavelike nature of holes within an 8-nm-Ge QD yields clear I_D plateaus and G_D peaks, which are a signature of adding or subtracting one hole to or from the QD through resonant energy levels. The nonperiodic G_D peaks originates from the interplay of inhomogeneous one-particle energy levels (E_j) and particle Coulomb interactions (E_j + U_{ij}, where U_{ij} denotes intra- or inter-level charging energies) in the Ge QD. Remarkably we observed negative differential conductance (NDC) phenomenon from the first G_D peak at $V_D \cong$ -40 mV when V_G = 0 and -0.2 V, whereas the feature of NDC disappears at high V_G for V_D < 0 and is not observable for the case of V_D > 0 even if V_G is small. This probably originates from the incompleted silicidation of the p^+-poly layer, leading to the band width of source electrode being not wide enough to cover energy levels of E_1 and E_1 + U_1.

To further clarify the tunneling current of Fig. 2 arising from discrete energy levels of the Ge QD, the Coulomb oscillatory current with respect to V_G and V_D is studied. When V_D < 30 mV, there are two oscillatory current peaks within the experimental V_G region (Fig. 3(a)). The first peak at V_G = -1.37V refers to carriers tunneling through the ground state (E_1), and the second peak at -2.25V arises from hole overcoming the charging energy of E_1 + U_1. Notably when V_D = -6 and -8mV, the first current peak exhibits a respective peak to valley ratio of 20 and 10 with extremely low leakage (<10^{-15} A). A three-dimensional I_D plot as functions of V_D and V_G (Fig. 3(b)) provides a comprehensive picture of how gate and drain influencing

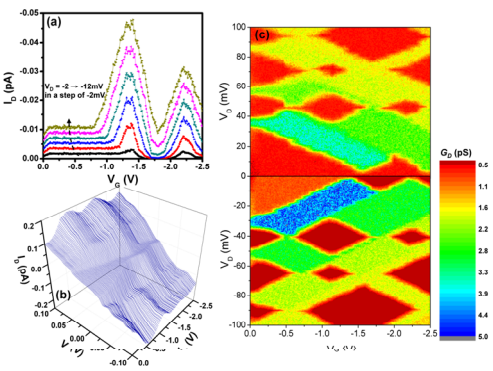

Figure 3 (a) I_D-V_G characteristics, (b) I_D-V_D-V_G , and (c) G_D contour plot of Ge QD SHT at T = 120 K.

charge tunneling through the Ge QD.

The experimental I_D-V_D and G_D-V_D characteristics reveal strong quantum mechanics effects imposed upon charges within the QD, making it possible to resolve the electronic structure of the Ge QD. Fig. 3(c) illustrates distinct Coulomb diamonds appear and each diamond represents one additional charge tunneling through one-particle energy levels (E_j) or overcoming particle Coulomb interactions. The slopes of the diamond correspond to the capacitance ratio among source, drain, and gate [21]. The experimental capacitance ratios of C_d : C_s : C_g = 18.9 : 21.8 : 1 suggests the gate modulation factor $\alpha = C_g/(C_d + C_s + C_g)$ of 0.0234, so the estimated single-electron addition energy for ground state is 36.5 meV by multiplying the peak V_G spacing and the gate modulation factor. The nonhomogeneous Coulomb diamond again suggests that the charging energies for overcoming the Coulomb interactions are likely less than the energy level separations because of large energy level separation within a 8-nm-Ge QD resulting from large dielectric constant and small effective mass.

4. Conclusions

Using the fidelity of spacer layer deposition and pattern-dependent SiGe oxidation, we precisely placed a single Ge QD among nano-electrodes through symmetrical tunnel barriers of Si_3N_4/SiO_2 in a self-organized approach, which offers a promising solution for the realization of effective SHTs over the conventional lithographic technique. The Ge QD SHT exhibits clear Coulomb staircase and Coulomb diamond characteristics so that we are able to resolve the electronic structure of the QD.

Acknowledgements

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References

[1] M. Saitoh, H. Harata, and T. Hiramoto, *IEDM Tech. Dig.*, (2004), pp.187–190.

[2] K. Yano, T. Ishii, T. Sano, T. Mine, F. Murai, T. Hashimoto, T. Kobayashi, T. Kure, and K. Seki, *Proc. IEEE*, 87 (1990) 4.

[3] K. Nishiguchi, A. Fujiwara, Y. Ono, H. Inokawa, and Y. Takahashi, *IEDM Tech. Dig*. (2004) pp. 199–202.

[4] T. Fujisawa, R. Tomita, T. Hayashi, and Y. Hirayama, *Science*, 312 (2006) 5780

[5] K. W. Chan, M. Mottonen, A. Kemppinen, N. S. Kai, K. Y. Tan, W. H. Lim, and A. S. Dzurak, *Appl. Phys. Lett*. 98 (2011) 21.

[6] A. Fujiwara, K. Nishiguchi, and Y. Ono, *Appl. Phys. Lett*. 92 (2008) 4. S.

[7] S. J. Shin, C. S. Jung, B. J. Park, T. K. Yoon, J. J. Lee, S. J. Kim, J. B. Choi, Y. Takahashi, and D. G. Hasko, *Appl. Phys. Lett*. 97 (2010) 10.

[8] K. H. Chen, C. Y. Chien, and P. W. Li, *Nanotechnology* 21 (2010)

[9] K. H. Chen, C. Y. Chien, W. T. Lai, T. George, A. Scherer, and P. W. Li, *J. Crystal Growth & Design* 11 (2011) 7.