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Integration of 1-bit CMOS Address Decoders and Single-Electron Transistors Operating at Room Temperature

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1. Introduction

Silicon-based single-electron transistors (SETs) operating at room temperature (RT) can realize future ultimately-high density LSIs thanks to their scalability and unique characteristics called Coulomb oscillation. While direct replacement of conventional CMOS logic circuits has been proposed, unconventional information processing circuits are also promising [1,2]. These novel circuits will be composed of a high-density array of SET cells with CMOS peripheral circuits such as address decoders to aggressively leverage scalability of SETs. For such applications, not only material compatibility but also fabrication process compatibility between SETs and CMOS are mandatory. So far, integrated circuit operation has already been demonstrated, where RT operating SETs were combined with a CMOS inverter [1] or a nMOS charge-pump [3]. However, integration of SETs with CMOS address decoders, which is necessary for high-density circuit using regularly-arrayed SETs, has not been achieved yet.

In this study, fabrication process of RT operating SETs is improved to achieve complete process compatibility with CMOS. 1-bit CMOS address decoders, which can be extended to larger address decoders, are integrated with SETs by the proposed process for novel information processing application realized by SET/CMOS fusion. Operation of a 1-bit address decoder combined with two SETs is demonstrated at RT for the first time.

2. Device Structure and Fabrication Process

In this study, RT operating SETs and n/pMOSFETs were integrated on a SOI substrate (Fig. 1). As shown in Fig. 2a, a SET has a nanowire (NW) channel, which is defined by electron-beam lithography and further narrowed by isotropic wet-etching and slight thermal oxidation [4]. The expected final width and height of a NW are less than 3 and 5 nm, respectively. In such an extremely-narrow NW, tunnel barriers originating from quantum confinement effect can be formed by shape fluctuations. When two sufficiently high barriers are formed closely in a NW channel, the device behaves as a SET rather than a NW FET (Fig. 2b).

In the conventional fabrication process of RT operating SETs, parasitic resistance and V_{th} of MOSFETs had to be considered to achieve better CMOS compatibility. To obtain extremely thin NWs without increasing parasitic resistance of MOSFETs, SOI around NW channels of SETs was partially thinned by LOCOS process, while the remaining regions were kept thick (Fig. 1). In addition, normally-off MOSFETs, which have high V_{th} (HVT) was realized by modulating work function of poly-Si gate electrodes, while no V_{th} control results in normally-on MOSFETs with too low V_{th} (LVT).

3. Circuit Configuration

For an information processing circuit with a large-scale array of SET cells, address decoders composed of row and column decoders are necessary to access a targeted cell, as is the case with memory circuits (Fig. 3a). A column decoder makes an electrical path to the selected bit-line. A row decoder activates the targeted cell on the bit-line and deactivates others by different word-line voltages. In this study, CMOS 2:1 multiplexers composed of 6 MOSFETs shown in Fig. 3 were used both as 1-bit column and row decoders.

4. Results and Discussion

By the improved fabrication process, RT operating SETs, nFETs (LVT, HVT) and pFETs (LVT, HVT) were successfully integrated (Fig. 4a,b). Thanks to suppression of parasitic resistance, MOSFETs exhibit reasonable current drivability (Fig. 4c). Comparable mobility to universal curve is also obtained (Fig. 4d). CMOS logic gates such as INV, NAND and NOR gates using HVT MOSFETs operate correctly with the supply voltage V_{DD} of 3.3 V (Fig. 5). These results indicate that the proposed fabrication process of RT operating SET is fully compatible with CMOS.

A CMOS 2:1 multiplexer is evaluated both as a 1-bit row and column decoders (Fig. 6). As shown in Fig. 7, the branch resistance of a 1-bit column decoder is as small as 1.1 kΩ when the branch is selected by the selection signal SEL, and the resistance ratio between selected and unselected branches is more than 10^8. Fig. 8 shows that a row decoder can correctly transfer one of the two input voltages to the output port when input voltages are below V_{DD}.

Finally, circuit operation is demonstrated at RT, where SETs and 1-bit CMOS row or column decoders are integrated (Fig. 9a, Fig. 10a). As shown in Fig. 9a, two different input ramp voltages were given to the SET through the 1-bit row decoder. The output current of the SET reflects only selected one of the two input voltages as shown in Fig. 9b. This means that input voltage to a SET cell is successfully switched by a CMOS row decoder.

A 1-bit column decoder was combined with a 1x2 array of SETs (Fig. 10a). In the output current of the array, only Coulomb oscillation peak of selected SET appears while that of unselected one does not, under given select signal SEL. In other words, an integrated CMOS column decoder realizes access to a targeted cell in an array of SETs. These results open up the possibility of novel information processing realized by SET/CMOS fusion.

5. Conclusions

Proposed CMOS compatible fabrication process of SETs has realized integration of SETs and basic CMOS circuits. Operation of circuits has been successfully demonstrated at room temperature, where SETs and a CMOS 1-bit row or column decoders are integrated.

Acknowledgements

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References

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[3] M. Nozue *et al*, *Proc. of Int'l Conf. on Ultimate Integration of Silicon* (2012) 201.
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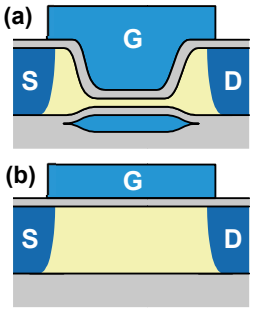


Fig. 1 Device structures of (a) SET and (b) MOSFET. Both devices are simultaneously fabricated on a SOI wafer.

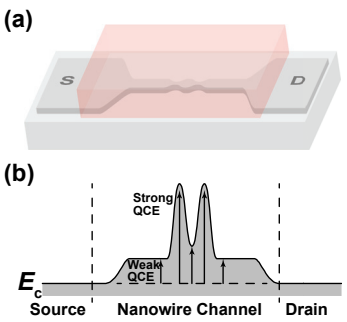


Fig. 2 (a) Schematic and (b) energy band diagram of a NW channel SET. Randomly formed shape fluctuations in a channel yield tunnel barriers and dots by quantum confinement effect (QCE).

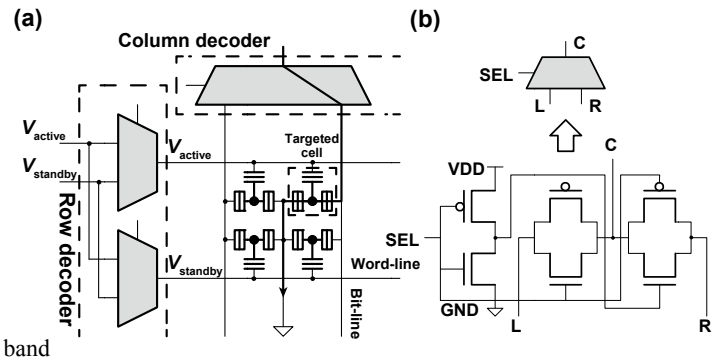


Fig. 3 (a) Schematic of a circuit composed of row and column decoders and an array of floating-gate SETs as an example of SET/CMOS fusion. (b) Implementation of a CMOS 2:1 multiplexer, which can be used for 1-bit column and row decoders.

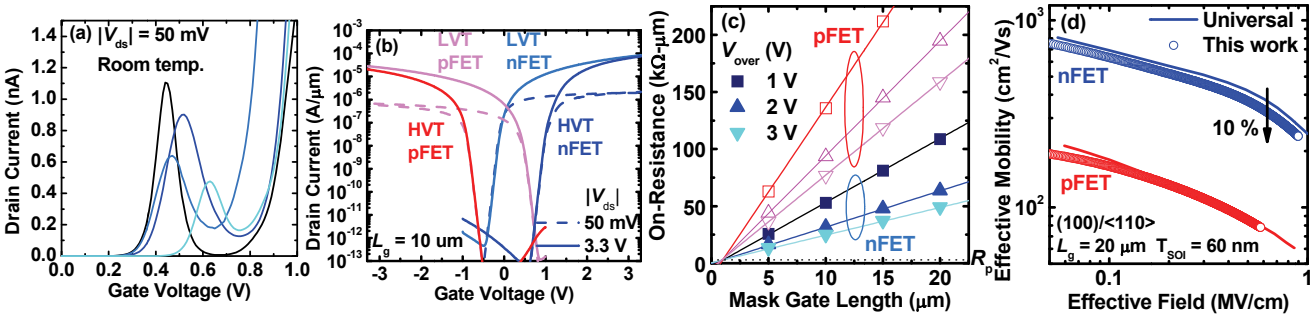


Fig. 4 Measured I_d-V_g characteristics of (a) SETs and (b) MOSFETs at room temperature fabricated by the proposed process on the same wafer. (c) On-resistance of MOSFETs as a function of mask gate length, which indicates small parasitic resistance (about 3 kΩ-μm) compared to channel resistance. (d) Effective mobility of MOSFETs. Comparable mobility to universal curve is observed in both nFET and pFET.

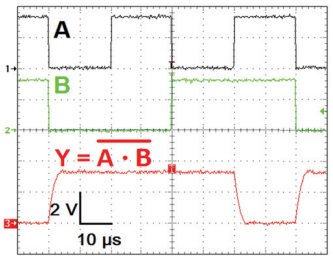


Fig. 5 Measured waveform of a CMOS NAND gate at 3.3 V V_{DD}, which is integrated with SETs on the same wafer.

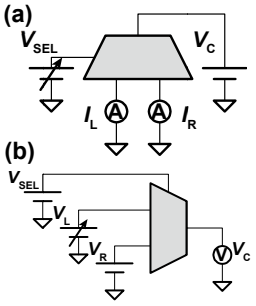


Fig. 6 Port assignments of CMOS 2:1 multiplexers as 1-bit (a) column and (b) row decoders. VDD and GND are omitted.

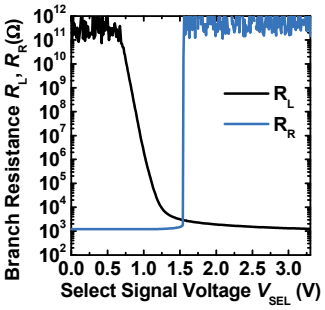


Fig. 7 Measured branch resistance of a 1-bit column decoder. Branch resistances are defined by $R_{L,\,R} = V_C / I_{L,\,R}$. High resistance ratio between branches is obtained.

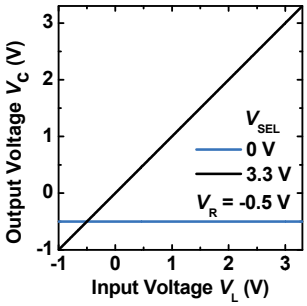
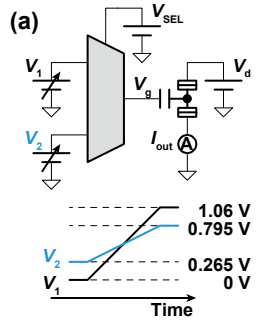


Fig. 8 Measured output voltage of a 1-bit row decoder. Ramp and fixed input voltages are given and selected one is correctly transferred.



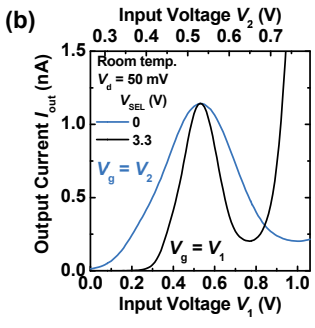
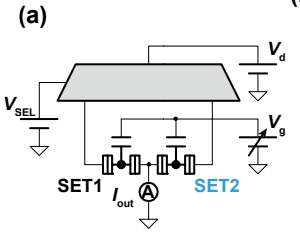


Fig. 9 (a) A circuit composed of a 1-bit row decoder and a SET whose gate voltage is fed through the decoder. (b) Measured output current of the SET at RT. Output is changed by the select signal SEL indicating that one of the two input voltages is selectively applied to the gate.



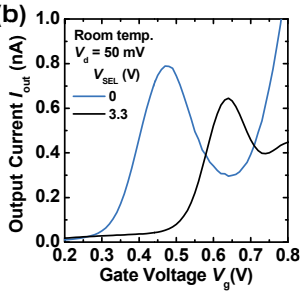


Fig. 10 (a) A circuit composed of a 1-bit column decoder and a 1x2 array of SETs whose drain voltage is supplied though the decoder. (b) Measured output current of the array of SETs at RT. Only Coulomb oscillation peak of a selected SET is observed in the output current.