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Observation of charging and discharging effects of dopant atoms in nanoscale lateral *pn* junction by Kelvin probe force microscope

Roland Nowak[1,2], Miftahul Anwar[1], Daniel Moraru[1], Takeshi Mizuno[1], Ryszard Jablonski[2], and Michiharu Tabe[1]

[1]Research Institute of Electronics, Shizuoka University, 3-5-1 Johoku Hamamatsu 432-8011, Japan
TEL/FAX: +81-53-478-1335; e-mail: nowak@rie.shizouka.ac.jp
[2]Division of Sensors and Measuring Systems, Faculty of Mechatronics, Warsaw Univ. of Technol., Poland

1. Introduction

Properties of individual dopant atoms, like ionization energy [1] or shape of dopant-induced confining potential well [2], depend on impurity location within the silicon lattice. Therefore, it is very important to know precisely the location of dopant atoms in the device structure. By using Kelvin probe force microscope (KFM) [3], we reported the observation of single dopants [4] and electron charging in donors [5,6] in nanoscale silicon-on-insulator field effect transistors (SOI-FETs), as presented in Fig. 1(a).

Besides the transistor, another important building block for LSI technology is the *pn* junction [7]. According to theoretical predictions, two-dimensional *pn* junctions, fabricated in thin semiconductor layers, exhibit interesting properties [8,9]. Yet, a small number of experimental papers, related to nanoscale lateral *pn* junctions, have been reported [10].

In this work, we measure nanoscale lateral *pn* junctions by KFM. Potential profile is significantly different from bulk *pn* junctions and originates from the two-dimensional nature of our device. In the depletion layer region, where, according to the *pn* junction theory, it is expected to see ionized dopants, we systematically observed noisy features, as shown in Fig. 1(b). This finding is ascribed to dynamic, random charging and discharging of donors and acceptors, which hinders the measurement of bare dopant potentials.

2. Potential profile and charging and discharging effects of dopants in the depletion layer

Experimental setup of the KFM measurement and SOI *pn* junction structure are schematically shown in Fig. 2. Based on fabrication process, it is expected that top-silicon layer is thinner than 10 nm. Backgate voltage, V_{BG}, was set to 0 V. *n*-type pad, doped with phosphorus donors ($N_D \approx 5 \times 10^{17}$ cm^{-3}), was grounded. To the *p*-type pad, doped with boron acceptors ($N_A \approx 1 \times 10^{18}$ cm^{-3}), negative voltage (V_{REV}) was applied, i.e., the junction was reversely biased. A grounded cantilever scans over the device surface at constant height. Scan area was located within the silicon constriction between the two pads. A dc-voltage (V_{KFM}), applied in order to nullify electrostatic force between tip and sample, corresponds to the electronic potential.

We measured *pn* junction potential profile at low temperature, 15 K. Figures 3(a)-(c) show KFM images taken at different values of applied V_{REV}. We found a noisy region between the flat-potential *n*- and *p*-type pads. This region can be identified as the depletion layer, since its width linearly depends on applied voltage, as shown in Fig. 4, in good agreement with theoretical prediction for 2D *pn* junctions [8].

Noise within the depletion layer is ascribed to random charging and discharging of dopants. For clarifying this point, we estimated carrier dwell time from the measured time of individual noise features. At low temperature, carrier dwell time is $10^0 - 10^1$ s, which corresponds to ionization energy of several tens of meV [11], consistent with shallow dopant properties. At room temperature, dwell time is in the range of $10^{-2} - 10^{-3}$ s, which gives ionization energy larger than 100 meV. This indicates that some dopants in the depletion layer are deeper-level phosphorus and boron atoms, i.e., their ionization energies are enhanced compared to the bulk value of 44 meV. This effect is expected in case of nanostructures, where dielectric confinement and quantum size effect become dominating [1].

We present averaged potential line profile in Fig. 3(d) for V_{REV} = -1 V. Potential difference between pads is around 150 mV. This relatively small value is probably due to the voltage drop in the silicon region outside of the junction. More importantly, the measured potential profile shows remarkable difference compared with bulk *pn* junction. Unlike in the case of ordinary *pn* junction, electric field strongly penetrates outwards from the thin depletion layer [Fig. 5(a)]. This particular electric field distribution in the depletion layer leads to the enhancement of the potential in this region, as schematically depicted in Fig. 5(b).

We finally focus on the depletion layer boundaries, at low temperature [Fig. 6(a)] and at room temperature [Fig. 6(b)]. Shifts of the edges, marked by dashed white lines, within the range of 10 nm, are observable. These shifts are most likely caused by ionization and neutralization of outermost dopants. An ionized dopant contributes to the depletion layer [Fig. 6(c)]. However, when it captures an electron, the depletion layer edge is shifted [Fig. 6(d)].

3. Conclusions

We measured nanoscale lateral *pn* junctions by KFM. The observed potential profile originates from electric field expansion outwards from the depletion region located in the thin Si layer. We found that noise features observed in the depletion region at room temperature are the result of charging and discharging of phosphorus and boron dopants, having deeper energy levels than in bulk. These results show ultimate differences between bulk and nanoscale *pn* junctions, essential for nanoelectronics development.

References

[1] M. Diarra *et al.,* Phys. Rev. B, **75**, 045301 (2007).
[2] G. P. Lansbergen *et al.,* Nature Phys. **4**, 656 (2008).
[3] M. Nonnenmacher *et al.,* Appl. Phys. Lett. **58**, 2921 (1991).
[4] M. Ligowski *et al.,* Appl. Phys. Lett. **93**, 142101 (2008).
[5] M. Anwar *et al.,* Jpn. J. Appl. Phys. **50**, 08LB10 (2011).
[6] M. Anwar *et al.,* Appl. Phys. Lett. **99**, 213101 (2011).
[7] S. M. Sze, *Physics of Semiconductor Devices,* 2nd ed. (John Wiley & Sons, New York, 1981).
[8] S. Petrosyan *et al.,* Appl. Phys. Lett. **84**, 3313 (2004).
[9] A. S. Achoyan *et al.,* Semiconductors **36**, 8 (2002).
[10] D. Reuter *et al.,* Appl. Phys. Lett. **86**, 162110 (2005).
[11] D. P. Foty, Cryogenics **30**, 1056 (1990).

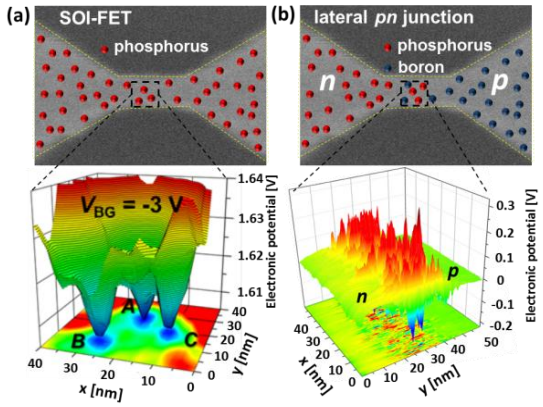

Fig. 1. (a) Observation of individual dopants by KFM at low temperature (15 K). (b) Measurement of nanoscale *pn* junction, in which the noisy region corresponds to the depletion layer.

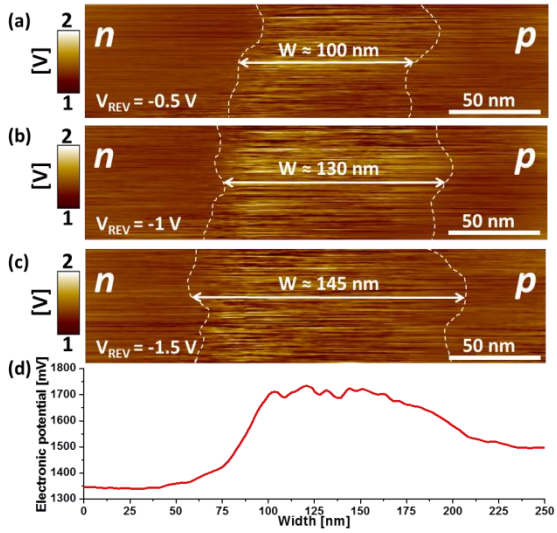

Fig. 3. (a)-(c) KFM images taken at 15 K for different reverse biases: -0.5, -1 and -1.5 V, respectively. Depletion layer (noisy area in the central part, delineated by dashed curves) expands at larger reverse biases. (d) Averaged potential profile from (b).

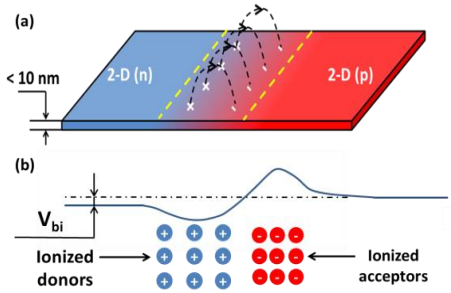

Fig. 5. (a) Schematic representation of electric field expansion from the depletion layer, reason for potential modulation in the depletion layer. (b) Dipole-like arrangement of ionized donors and acceptors, causing a potential profile similar to the experimental observation.

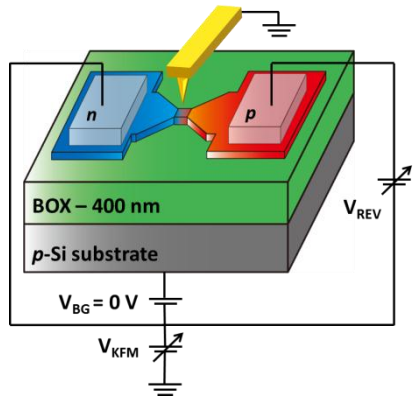

Fig. 2. Device structure and KFM measurement setup. Scan area was located in the center of the constriction between *n*- and *p*-type silicon pads.

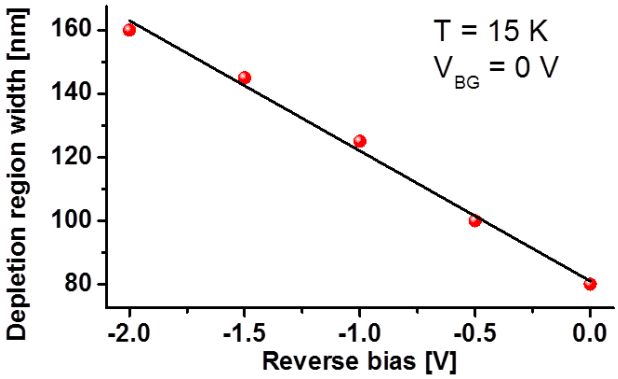

Fig. 4. Width of depletion layer as a function of reverse bias. Linear dependence on applied voltage is consistent with theoretical prediction for 2D *pn* junction [8].

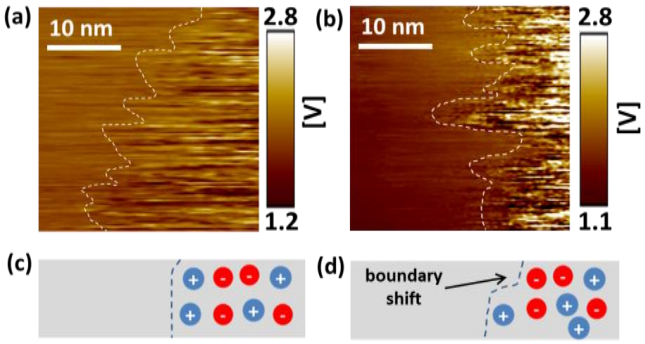

Fig. 6. Depletion layer edges at 15 K [(a)] and at room temperature [(b)]. In both cases, boundary fluctuations within 10-nm range can be seen, reflecting charging/discharging of outermost dopants, as schematically shown in (c) and (d). Initially ionized donor atom contributes to the depletion layer [(c)], but the depletion layer edge shifts when the donor becomes neutralized [(d)].