Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials, Kyoto, 2012, pp953-954

Enhanced memory performance using forming free $IrO_x/GdO_x/W$ crossbar resistive switches

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1. Introduction

Due to conventional flash memory approaching its scaling limits, the resistance random access memory (ReRAM) has attracted wide attention for non-volatile memory application because of its simple structure, low operating power, fast switching speed, high-density, multilevel charge storage, and scalability potential [1]. Plenty of materials, such as binary metal oxides, perovskite oxides, rare-earth metal oxides has been studied by several groups [2-5]. But the rare-earth metal oxide Gd_2O_3 as a switching material in ReRAM has been discussed in frequently [6,7]. In our previous study, we reported the formation polarity dependent GdO_x resistive switching memory with high current compliance (I_{CC}) of 1mA [7]. In this study, formation free resistive switching memory with a small I_{CC} of 50μA in an $IrO_x/GdO_x/W$ crossbar architecture is reported. This memory device has excellent dc/ac endurances of $>10^4$ cycles, stable multi-level operation, and data retention of 10^4 s at 85°C.

2. Experiment

After conventional RCA cleaning of p-Si wafer, 200nm-thick SiO_2 layer was grown by wet oxidation process. Then, W as a bottom electrode (BE) was deposited by RF sputtering. A device size of 4×4 μm^2 was patterned by optical lithography and etching process. Then GdO_x as a switching material was deposited by E-beam evaporator. IrO_x as a top electrode (TE) was deposited by RF sputtering. Finally, lift-off was performed to obtain the final device. The crossbar memory device was annealed at 400°C in N_2 ambient for 10min.

3. Results and discussion

Fig.1 shows the schematic view of our $IrO_x/GdO_x/W$ cross-point memory device. Inset figure shows the optical microscope image of our cross-point memory device. Each layer is clearly observed from the HRTEM image (Fig. 2). Thickness of GdO_x film is approximately 17.5 nm. EDX spectra confirm the presence of expected elements of Ir, Gd, W and O in respective layers (Fig. 3). Typical bipolar current-voltage (I-V) characteristics for both as deposited and anneal sample are shown in Fig.4. The direction of I-V curve with a current compliance (Icc) of 300 μA are indicated as follows 1→4. Initially, no formation process is needed to initiate the resistive switching behavior. The surface roughness of the W BE and the pre-existing defects in the GdO_x film during deposition are the key point of our forming free resistive switching, owing to the higher defects in percolation length. That's why formation free resistive switching memory is obtained. The annealing device is showing higher high resistance state (HRS) as compared to the as-deposited one, which is unwanted defects annealed out, resulting in a higher resistance ratio (HRS/LRS). The annealed device shows repeatable consecutive 100 switching cycles with a small operation voltage of ±3V. To elucidate the current conduction mechanism, I-V curve was re-plotted in log-log scale (Fig.5). Both low resistance state (LRS) and HRS exhibit trap-controlled space-charge-limited-current (TCSCLC) conduction mechanism, which consists ohm's law ($I \propto V$) in low voltage region and child's law ($I \propto V^2$) in high voltage region. The switching mechanism is based on the formation of oxygen vacancy conducting path or Gd-rich filament and rupture by oxidation through O^{2-} migration. When positive voltage applied on the TE, Gd-O bonds break easily because of higher defects and O^{2-} ion attracted to the TE/GdO_x interface. The device switches from HRS to LRS. When negative bias applied on the TE, O^{2-} ion are migrated from the TE/GdO_x interface, resulting in ruptured the filament, and the device switches from LRS to HRS. Interfacial oxygen-rich layer at TE/GdO_x plays series resistance, which controls the O^{2-} ions migration, as well as repeatable switching cycles are observed. Fig.6 shows the multi-level I-V curve with I_{CCs} of 50-300 μA. With increasing the current compliance, the conducting path through the GdO_x layer becomes more conducting. That's why with increasing the I_{CC}, resistance level in the low resistance gradually decreases. Fig.7 shows excellent multi-level retention characteristics with I_{CCs}. After 10^3 s., the resistance ratio (HRS/LRS) for 50, 100, and 300 μA are approximately 10, 100, and 500, respectively. Fig. 8 shows the multi-level operation with variation of stop voltages. When negative bias applied on the TE, O^{2-} are migrated and oxidation length of the conducting path at the TE/GdO_x interface increases with increasing the negative voltages. That's why current level in the high resistance state gradually decreases. Fig. 9 shows the multi-level retention characteristics with variation of stop voltages. Obviously, the resistance ratio increases with increasing the stop voltages. Fig. 10 shows the AC endurance of 10^4 cycles. Both resistance states were read out at +0.2V. Program/erase voltages are +2.8V/-2.5V. After 10^4 cycles, resistance ratio is approximately ~30. Fig. 11 shows the read endurance of our memory device. After 10^5 cycles, a stable resistance ratio of ~ 60 is obtained. Fig. 12 shows the retention characteristics of the cross-point memory device at room temperature (RT) and 85°C. The LRS at 85°C is increased. This is typical electronic transport behavior through Gd-rich metallic filament, which is based on the phonon scattering phenomena. However, resistance level at HRS decreases with increasing temperature indicating the defective GdO_x film. The defective GdO_x film is also observed from the capacitance-voltage measurement (not shown here). Both resistance states were read out at +0.2V. After 10^4 s data retention, a high resistance ratio of ~ 300 at RT and resistance ratio of ~ 30 at 85°C are obtained. Memory device is showing very stable retention characteristics with high resistance ratio which is very useful for future nanoscale non-volatile 3D memory application.

4. Conclusion

Novel memory device in an $IrO_x/GdO_x/W$ cross-point structure has been investigated. Each layer clearly observed from HRTEM image. EDX spectra confirm the presence of expected elements. Memory device is showing forming free, good endurance, excellent multi-level operation with variation of current compliance as well as variation of stop voltage, good AC endurance of 10^4 cycles, excellent read endurance of 10^5 cycles, and stable data retention of 10^4 s 85°C with a high resistance ratio. This memory device has great potential for future nanoscale non-volatile 3D architecture.

Acknowledgment

This work was supported by National Science Council (NSC), Taiwan, under the contract no. NSC-98-2221-E-182-052-MY3.

References

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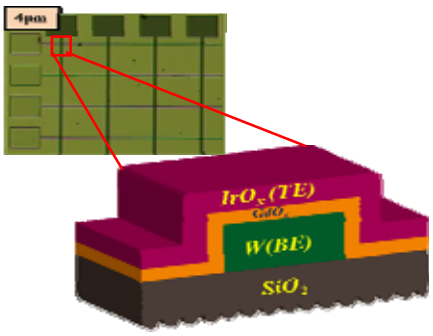

Fig. 1 Optical image and schematic view of the crossbar resistive switching memory devices using $IrO_x/GdO_x/W$ structure are shown. The device size is 4x4 μm^2.

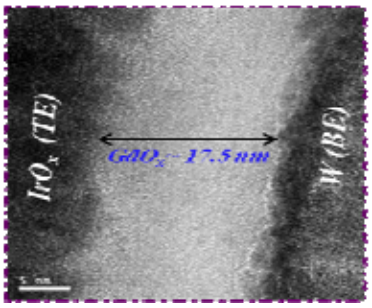

Fig. 2 Cross-sectional HRTEM image of $IrO_x/GdO_x/W$ crossbar memory device. Thickness of GdO_x layer is ~ 17.5 nm.

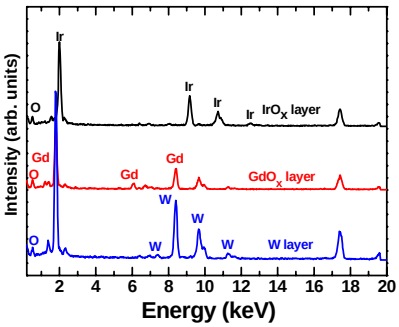

Fig. 3 Energy dispersive X-ray spectra (EDX) shows Ir, Gd, W, and O elements from Fig. 2. It proves layer-by-layer structure with presence of GdO_x resistive switching layer.

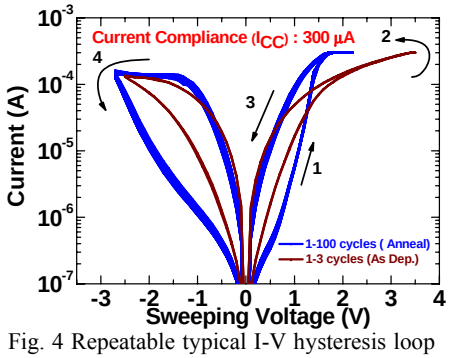

Fig. 4 Repeatable typical I-V hysteresis loop of our $IrO_x/GdO_x/W$ crossbar memory device is observed after annealing. A low operation voltage of < ±3V is applied to achieve repeatable and reproducible cycles.

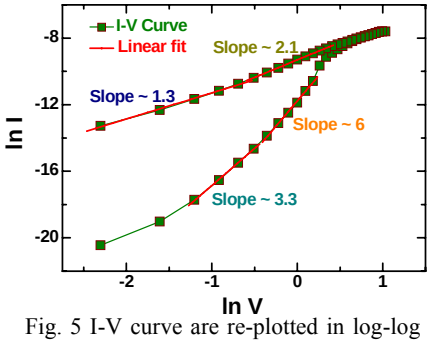

Fig. 5 I-V curve are re-plotted in log-log scale. Both resistance state exhibits trap controlled space charge limited current conduction mechanism.

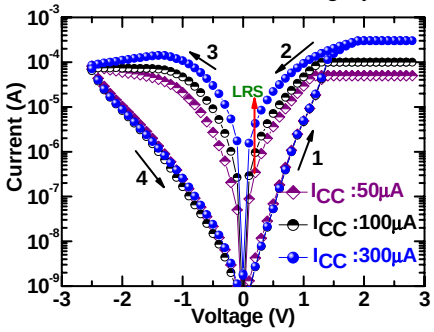

Fig. 6 I-V hysteresis loop of $IrO_x/GdO_x/W$ crossbar memory device with the variation of I_{CC} from 50-300 μA. Multi-level data storage is observed.

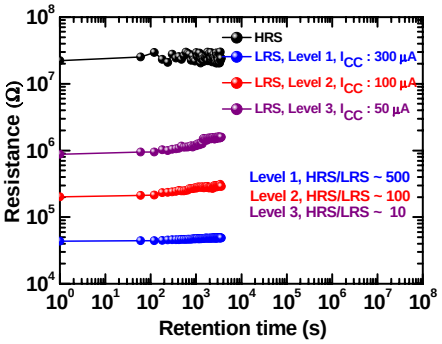

Fig. 7 Excellent multilevel retention characteristics of $IrO_x/GdO_x/W$ crossbar memory device with different current compliances.

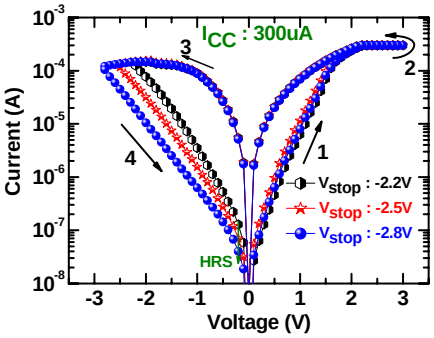

Fig. 8 I-V hysteresis loop with the variation of stop voltage of our $IrO_x/GdO_x/W$ crossbar memory device. The HRS increases with increasing the negative voltages.

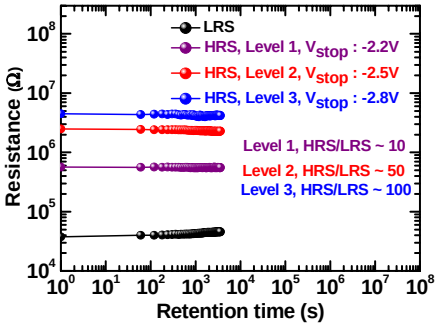

Fig. 9 Excellent multilevel retention characteristics with the variation of stop voltage of our $IrO_x/GdO_x/W$ crossbar memory device are observed.

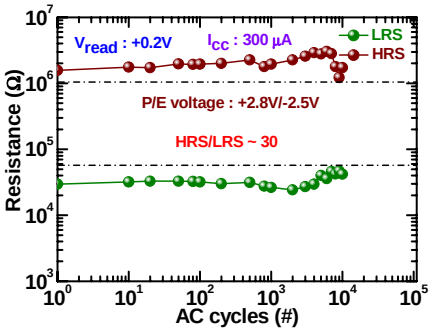

Fig.10 Excellent ac endurance of $>10^4$ cycles of our $IrO_x/GdO_x/W$ memory device. The resistance states were read out at +0.2V.

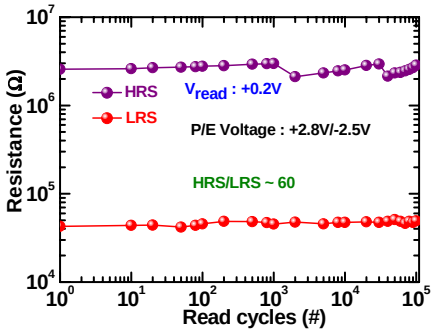

Fig.11 Good read cycles of 10^5 cycles of our crossbar memory device. Both resistance states were read out at +0.2V.

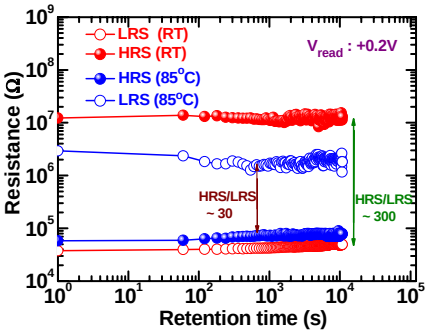

Fig. 12 Excellent retention characteristics of $>10^4$ s at RT and 85°C of our $IrO_x/GdO_x/W$ crossbar memory device are reported.