

Fabrication and Characterization of p-Channel Si Double-Quantum-Dot Structures

Ko Yamada^{1*}, Tetsuo Koderu^{1,2,3}, Tomohiro Kambara¹, Yukio Kawano¹, Shunri Oda¹

¹ Quantum Nanoelectronics Research Center, Tokyo Institute of Technology, 2-12-1 O-okayama, Meguro-ku, Tokyo 152-8552, Japan

² Institute for Nano Quantum Information Electronics, The Univ. of Tokyo, 4-6-1 Komaba, Meguro-ku, Tokyo 153-8505 Japan

³ PRESTO, Japan Science and Technology Agency (JST), 4-1-8 Honcho Kawaguchi, Saitama, 332-0012, Japan

*Phone: +81-3-5734-2542, Fax: +81-3-5734-2542, E-mail: yamada.k.av@m.titech.ac.jp

1. Introduction

Electron spins are a promising candidate for solid-state quantum bits (qubits) [1]. Electron spins in Si are expected to have a long coherence time owing to almost no nuclear spins. Furthermore spin-orbit interaction of holes is smaller than that of electrons, because valence band have small p-like symmetry compared to conduction band in Si. Therefore hole spins in Si quantum dots (QDs) presumably have much longer coherence time. Then, we focused on p-type Si QDs.

Coulomb oscillation in p-type Si single QDs has been reported [2]. However, there are no reports of transport properties through lithographically-defined p-type Si double QDs (DQDs).

In order to manipulate hole spins in DQDs, it is preferable to reduce the number of holes in each QD down to one, which can be detected by measuring charges using a charge sensor (CS) such as a single hole transistor (SHT).

In this paper, we present measurement results of Coulomb oscillation and Coulomb diamond in a p-type Si single QD and honeycomb-like charge stability diagrams of p-type Si DQDs. We also demonstrate the detection of charge transition the DQD using SHT as CS.

2. Device structure

Schematic image of our device structure (Device B) on silicon-on-insulator (SOI) is shown in Fig. 1(a). Si DQDs, an SHT and side gates (SG1, SG2 and SG3) are fabricated by electron beam lithography and dry etching. The side gates are used for controlling potential of each QD and modifying tunnel rates through each potential barrier. Constricted regions controlled to be about 10 nm width, by thermal oxidation after dry etching, are potential barriers for the Si DQDs and SHT. We implant BF_2^+ in SOI layer at source (S) and drain (D) regions. The peak concentration is $8 \times 10^{19} \text{ cm}^{-3}$. We induce holes in the DQD and SHT by applying negative voltage to a back gate (BG).

Figure 1 (b) and (c) show scanning electron microscope (SEM) images of Device A and B, respectively. Device A is the p-type Si SHT. Device B is the p-type Si DQDs with SHT. The thicknesses of an SOI layer and buried-oxide (BOX) are 33 nm and 145 nm, respectively.

3. Results and discussion

At first, we swept back gate voltage V_{BG} . Figure 2 (a) and (b) show I_D - V_{BG} characteristics of Device A measured at 300 K and 4.2 K, respectively. Figure 2 (a) shows p-channel MOSFET characteristic. Figure 2 (b) shows Coulomb oscillation at negative V_{BG} . These results indicate that we observe the tunneling of single holes in Device A at 4.2 K.

Figure 3 shows Coulomb diamond, which is obtained

by sweeping side gate voltage V_{SG} from 0 V to 1 V and source-drain voltage V_{DS} from -20 mV to 20mV when V_{BG} is fixed at -5V. Charging energy is estimated at 16meV from averaged Coulomb diamond sizes. Diameter of the QD is evaluated as 40 nm from the charging energy. This value almost corresponds to the diameter of the QD estimated from the SEM image in Fig. 1(b). This means that we successfully fabricated lithographically-defined p-type Si QDs.

Figure 4 (a) and (b) show I_D - V_{BG} characteristics of the SHT and DQD measured for Device B at a temperature of 4.2 K, respectively. Coulomb oscillations are observed for both the SHT and DQD.

Figure 5 shows charge stability diagram of DQD and SHT measured for Device B. Figure 5 (a) shows dI_{DQD}/dV_{SG1} in the plane of V_{SG1} and V_{SG2} . Two lines with different slope in Fig. 5 (a) make honeycomb structure, which is a typical behavior in DQDs. Figure 5 (b) shows a magnified plot of a dashed square region in Fig. 5 (a). We observe the two lines with different slopes as indicated by dotted line. Figure 5 (c) shows dI_{SHT}/dV_{SG1} in the plane of V_{SG1} and V_{SG2} , which is simultaneously measured with Fig. 5 (a). Figure 5 (d) shows a magnified plot of a dashed square region in Fig. 5 (c). We clearly observe the two line patterns with different slopes on top of the Coulomb oscillation of SHT itself. This result means that we succeeded in sensing of electronic state in the DQD using the SHT. Furthermore, the lines are not observed at the region of more positive side gate voltages, which indicates we might observe the few-hole regime.

4. Conclusions

We have investigated transport properties of p-type QDs. The Coulomb oscillation peaks and Coulomb diamond of hole transport was observed by measuring the single QD. Honeycomb-like charge stability diagrams were obtained by measuring the DQD. Furthermore we succeeded in charge sensing of the charge transitions in the DQD using the SHT as the CS. Therefore we successfully fabricated a p-type lithographically-defined DQD device using Si, for the first time.

Acknowledgements

This work was financially supported by KAKENHI (22246040, 24102703), JST-PRESTO, Yazaki Memorial Foundation for Science and Technology, and Project for Developing Innovation Systems of the Ministry of Education, Culture, Sports, Science and Technology (MEXT).

References

- [1] D. Loss and D.P. DiVincenzo, *Phys. Rev. A* **57** (1998) 120
- [2] Sejoon Lee, Kousuke Miyaji, Masaharu Kobayashi, and Toshiro Hiramoto, *Appl. Phys. Lett.* **92**, 073502 (2008)

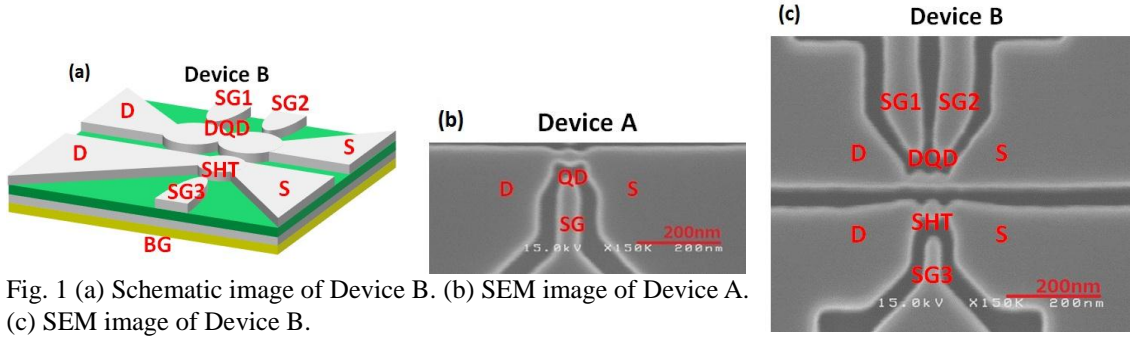


Fig. 1 (a) Schematic image of Device B. (b) SEM image of Device A. (c) SEM image of Device B.

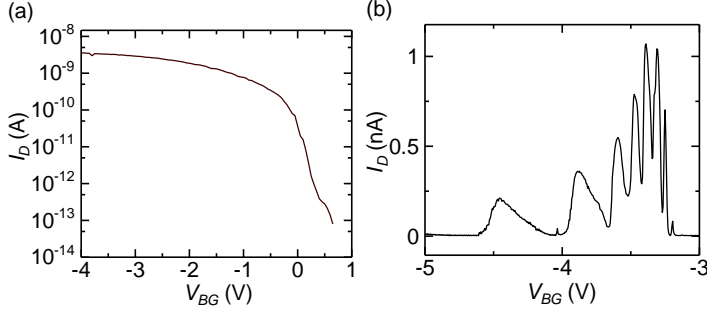


Fig. 2 I_D - V_{BG} characteristics of Device A measured at a temperature of (a) 300K and (b) 4.2K, respectively.

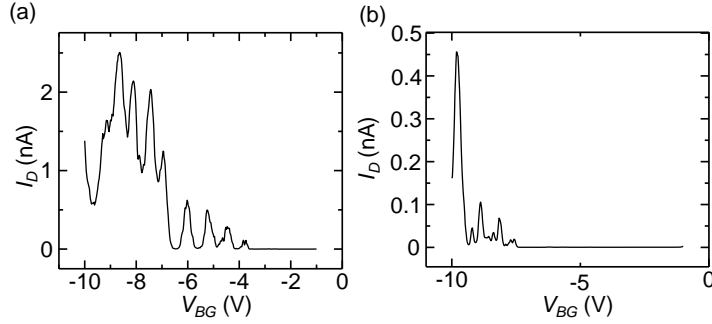


Fig. 4 I_D - V_{BG} characteristics of (a) SHT and (b) DQD of Device B.

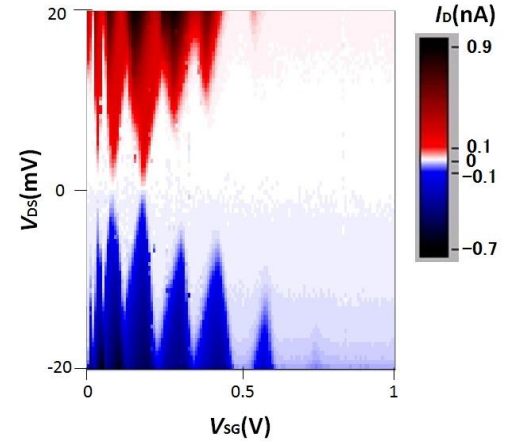


Fig. 3 I_D in the plane of V_{SG} vs V_{DS} measured for Device A. $V_{BG} = -5V$.

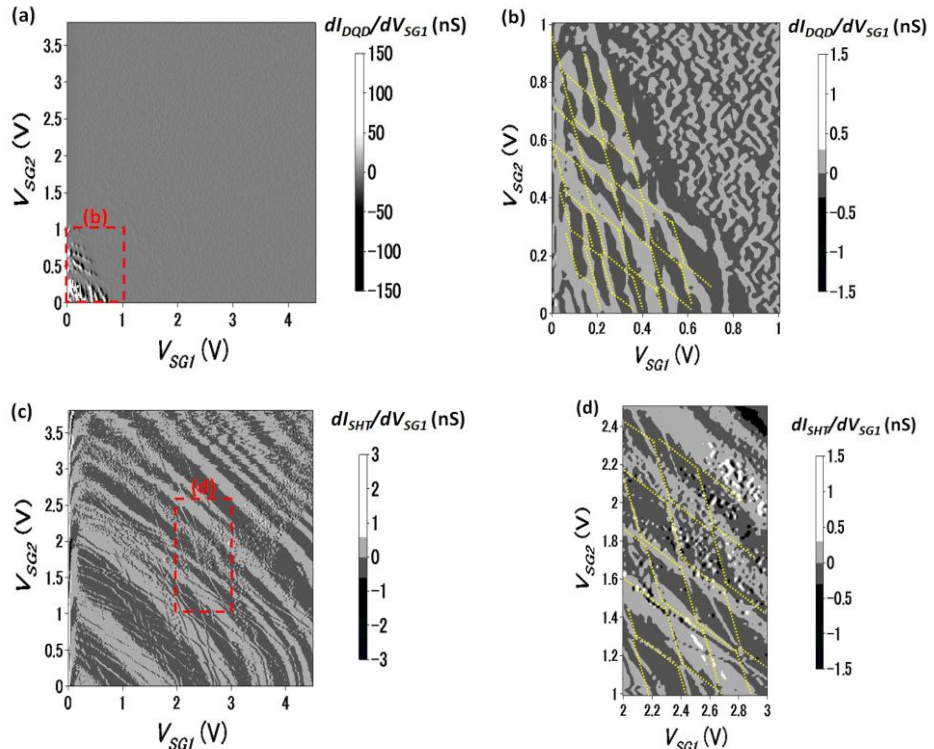


Fig. 5 Charge stability diagram of conductance of (a) DQD and (c) SHT, respectively. (b) and (d) Magnified plots of dashed square region in (a) and (c), respectively.