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Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials, Kyoto, 2012, pp989-990

# Spalling of thin Si layer by electrodeposit assisted stripping (EAS) process

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## 1. Introduction

Single crystalline Si(c-Si) has been used for many kinds of semiconductor devices including VLSI, sensors, and solar cell. Even though Si is one of abundant materials in the earth, it still very expensive, because high cost processes are required to guarantee its high purity and low defect density. Nowadays, the thickness of conventional c-Si substrate is 300~500μm, however the thickness reqired for photon absorption is about 50μm. Therefore if thin layer of Si film (~50um) can be consecutively detached from conventional Si wafers without generation of structural defects, we can drastically reduce the cost for the fabrication of Si solar cell.

Thin c-Si layer, which has ~50μm thickness, can be detached by electrodeposit assisted stripping (EAS) process. Upon electrodeposition process, the large lattice mismatch induces a strong stress field, which is released by the initiation and propagation of a crack parallel to the surface[1]. After lift-off thin Si film, the mother substrate can be reused.

In this study, Ni-P alloys with various current and phosphorus contents were electrodeposited from nickel chloride baths through additions of distinct amounts of $H_3PO_3$.

## 2. Experimental

*Internal stress analysis*

Ni and Ni-P thin films were electrodeposited from chloride baths. They contained 0.6M $NiCl_2$, 0.5M $H_3BO_3$ and 0-0.01M $H_3PO_3$. Boric acid was used as pH buffer. Ni and Ni-P film were galvanostatically electrodeposited at room temperature without stirring. The internal stress was measured by deflection method with a deposit stress analyzer.

*Si wafer lift-off*

The Si striping process is schematically described in Fig.1. Single crystalline silicon wafer with 500μm was used as a starting material. A Ti seed layer (50nm)/Ni seed layer (50nm) was deposited on the silicon substrate by sputtering for improving adhesion between substrate and electrodeposit. After cleaning the substrate by dipping in 10% HCl for 20 seconds, Ni and Ni-P alloys were electrodeposited at constant current density. Ni and Ni-P thin films induced the large stress to the Si substrate, then the deposited metal begun to pill off with few tenth micrometer of silicon film. After the striping, metal layer which induced an internal stress in the stripped Si films, were removed in metal-etching solution, resulting in a stress-free Si films.

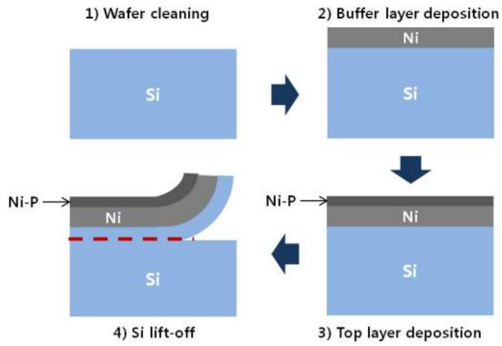
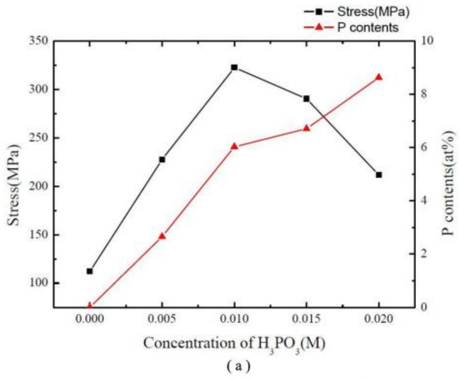



Fig. 1 The schematic of Si wafer lift-off by electrodeposition process.

## 3. Results and Discussion

Initially, the stress of Ni and NiP films were systematically investigated to find out the optimum condition of stress of metal electrodeposits for Si stripping. Figure 2(a) shows the dependence of film stress in Ni and Ni-P electrodeposits on the $P^{3-}$ ion concentration in the electrolytes. As $P^{3-}$ ion concentration increased from 0 to 0.01M, the film stress was increased from 110 to 320 MPa. However, when $P^{3-}$ ion concentration increased more than 0.01M, the film stress decreased, which might be caused the generation of micro-cracks in NiP layers. As $H_3PO_3$ concentration in the solution increased, phosphorus content of the deposit increased, which caused the deceasing of average grain size of crystallites. The microstructure of electrodeposited nickel is FCC system and the co-deposited phosphorus can be placed in octahedral interstitial sites of FCC Ni. During the electrochemical reduction of Ni, phosphorus atoms which placed on a Ni hinder crystal growth of Ni resulting in small grain size or even an amorphous structure, which causes the variation of the internal stress [2].

The effects of the current density on the film stress and P content in the films are represented on Fig.1 (b). As the current density increased from 5mA/cm$^2$ to 20mA/cm$^2$, the stress of the film was increased to maximum as 320Mpa. When current density was increased more than 20 mA/cm$^2$, the film stress was slightly decreased. The current density also affects to the grain size of electrodeposits, and generally the higher current density enhances the reduction of the grain size.



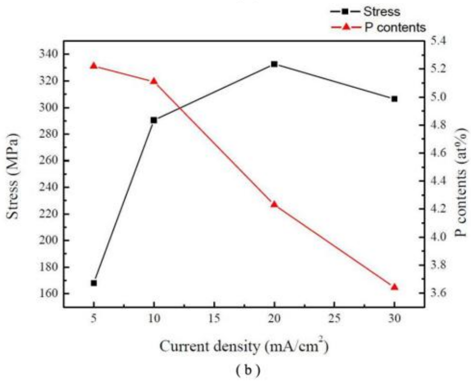




Fig. 2 Dependence of film stress on $H_3PO_3$ concentration (a) and the current density (b)

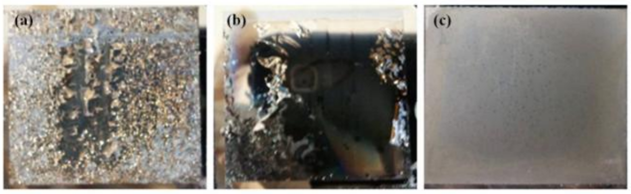



Fig. 3 Electrodeposited films in the 0.6M $NiCl_2$, 0.5M $H_3BO_3$, 0.01M $H_3PO_3$ bath at 20mA/cm$^2$ (a), at 5mA/cm$^2$ (b), and in the pure Ni bath at 5mA/cm$^2$ (c).

The film cracking behavior after individual Ni and Ni-P alloy film were electrodeposited on the Si wafer were shown in Fig.3. when NiP film with ~320Mpa of stress were deposited, the metal films were fractured in multiple pieces [Fig 3(a)]. If current density was decreased to 5mA/cm$^2$, the metal film only peeled off like a foil because of adhesion issue [Fig 3(b)]. When Ni was electrodeposited in the pure Ni bath at 5mA/cm$^2$ which is the lower stress condition (~69 Mpa), stable film was obtained, but the Si lift off did not occur [Fig 3(c)].

To obtain conformal Si lift off, two layers which have different internal stresses were consecutively electrodeposited as shown Fig 4. First, a 40 ㎛ of stress buffer layer was deposited to prevent seed layer fracturing, and then a 5 ㎛ of high stress layer is deposited to lift off the Si layer. Fig. 5 clearly shows the stripped Si layer and remained Si wafer after EAS process. The thickness of stripped Si layer was ~50um, and it was continuously bended because of high stress of metal layers. After removing the metal layer by metal etchant, perfectly flat Si layer could be obtained.


Fig. 4 The schematic of 2-layer-method.

Fig. 5 Pictures of 3.5x3.5 cm$^2$ ~50㎛ thin Si film along with the residual wafer after lift-off.

## 4. Conclusion

~50 um of Si layer was successfully stripped form single crystalline Si wafer by Electrodeposit Assisted Si Stripping (EAS) process. The 40㎛ lower stress layer, Ni was deposited as a buffer layer, then the higher stress layer, NiP was deposited to initiate the stripping of Si. As a result, a 50㎛ Si thin film was gradually stripped during the high stress layer deposition. EAS process can separate thin Si layer in room temperature condition, undesired structural defects caused by thermal expansion can be effectively minimized, which might allow the higher efficiency of solar cell.


## Acknowledgements

This work was supported by the New & Renewable Energy Technology Development Program of the Korea Institute of Energy Technology Evaluation and Planning grant funded by the Korea government Ministry of Knowledge Economy, and the Pioneer Research Center Program through the National Research Foundation of Korea (2010-0002231) funded by the Ministry of Education, Science and Technology (MEST).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## Appendix


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