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Fat damascene wires for high bandwidth routing in silicon interposer

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1. Introduction

System-In-Package (SIP) enables flexible and low cost integration of multiple components such as memory, logic or passives in a single package. However, SIP performances are today limited for high performances applications such as FPGA, processor or GPU in which high bandwidth communication between the elements of the system is required. The use of an intermediate carrier such as Silicon Interposer between IC chips and substrate resolve the bandwidth bottleneck by increasing the I/Os number. Indeed, Si Interposer combines fine pitch µBumps and high density routing for fast and high bandwidth interconnection between mounted chips. Low cost semi-additive electrochemical plating process (ECP) is often used for interposer routing processing [1]. Damascene process is an alternative allowing for an improved reliability (use of barrier between Cu and dielectric) and better line pitch scalability [2]. However, the use of thin lines characteristic of standard damascene technology such as 65 nm Back-End-Of-Line (BEOL), impact overall signal transmission performances because of their relative high resistance compare with ECP approach. In this work, impacts of Cu lines dimensions and line neighboring onto system bandwidth and crosstalk are first simulated. The output allows for optimal performances interposer damascene interconnect which process and characterization are described in a second part.

2. Impact of wiring parameters on signal integrity

For the transmission of high frequency signals, µstrip configuration including Cu signal lines and ground plane (GND) separated by SiO_2 dielectric layer were considered for interposer routing (Fig. 1a). Full transmission line model was used to provide wiring parameters range of interest to enable technology development (Fig. 1b). A single interposer transmission line of length ℓ and the equivalent properties of transmitter/receiver are described by their ABCD-matrix in eq. (1).

$$\underbrace{\begin{bmatrix} 1 & R_{TRAN} \\ 0 & 1 \end{bmatrix}}_{ABCD_{TRAN}} \times \underbrace{\begin{bmatrix} \cosh(\gamma\cdot\ell) & Z_0\sinh(\gamma\cdot\ell) \\ \sinh(\gamma\cdot\ell)/Z_0 & \cosh(\gamma\cdot\ell) \end{bmatrix}}_{ABCD_{CHANNEL}} \times \underbrace{\begin{bmatrix} 1 & 0 \\ j\omega C_{LOAD} & 1 \end{bmatrix}}_{ABCD_{RCV}} \quad (1)$$

Where:

$$Z_0 = \sqrt{\frac{R + j\omega L}{j\omega C}} \quad \text{And} \quad \gamma = \sqrt{(R + j\omega L) j\omega C}$$

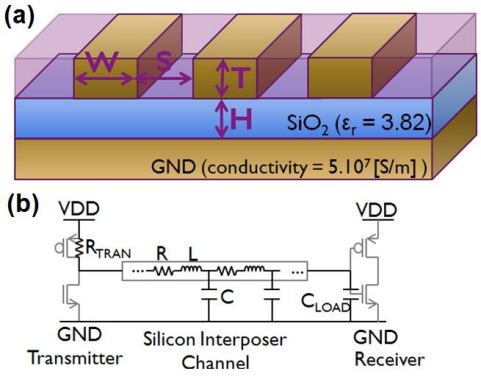

Fig1 (a) µstrip configuration of interposer transmission lines where W, T and S corresponds respectively to signal lines width, thickness and spacing, and H to dielectric (SiO_2) thickness.
(b) Full transmission line model of interposer channel.

Single line bandwidth is extracted from corresponding transfer function of eq.(1) in frequency domain. In the practical cases, multiple lines are integrated having W and S as shown in Fig. 1(a). When a routable space (bus width) is given, the number of channels can be estimated and system bandwidth is calculated by multiplying single line bandwidth and the number of channels. In the case of crosstalk, the mutual values between lines are considered by expanding eq.(1) to coupled transmission line theory and the crosstalk between aggress channel to victim channel is evaluated.
10 mm length lines with 5mm bus width were simulated by fixing V_{dd} to 1V, source resistance (R_{TRAN}) to 50 Ω and load capacitance (C_{LOAD}) to 500 fF. Interposer channel R, L and C were extracted based on wiring parameters and by fixing SiO_2 relative permittivity to 3.82 and Cu conductivity (Signal and GND) to 5.10^7 S/m. Total system bandwidth and crosstalk (red lines) were drawn simultaneously as a function of lines width W and spacing S on Fig.2(a) for a given line when T=1 µm and H=2 µm..

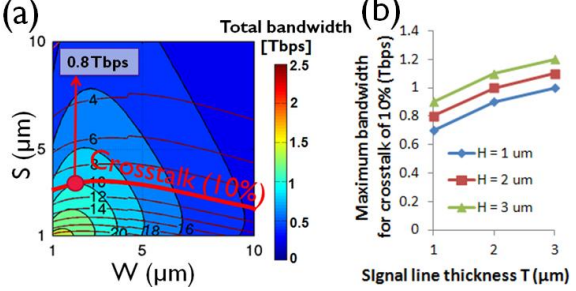

Fig. 2 (a) System bandwidth (color code in Tbps) versus crosstalk (red lines in %) as a function of lines width W and spacing S for a given line when T=1 µm and H=2 µm, respectively.
(b) Maximum bandwidth for a given crosstalk of 10% as a function of signal line thickness T and dielectric thickness H.

Fig.2(a) shows that maximum system bandwidth is obtained for low line pitch (space and width below 5 µm), where the number of channel which can be integrated in the 5 mm bus width is the maximum. However, by reducing line spacing, the crosstalk between channels logically increases as well. A tradeoff is then necessary between maximum system bandwidth and acceptable crosstalk value. By fixing the maximum crosstalk to 10%, then a maximum bandwidth of 0.8Tbps is reach according to the model for optimum line width W and spacing S of ≈ 2 and 3 µm respectively.

In order to investigate the process parameters, various signal line thickness T and dielectric thickness H values were assessed ranging from 1 to 3 µm with the same W and S. Fig.2(b) shows that the maximum system bandwidth for an acceptable crosstalk of 10% increases with signal line and dielectric thickness with a maximum of 1.2 Tbps for 3/3 µm. Due to technology constrains, fat line and dielectric thickness of 2/2 µm were however preferred for interposer BEOL processing, with line space/width between 1 and 5 µm (see part 3).

3. Process and characterization of fat damascene wires

Fat line development and characterization for interposer application were carried out by processing µStrip structures. They consist in a stack of 1 µm Cu Ground plane (GND), 2 µm dielectric and 2 µm Cu signal lines with a width ranging from 1 to 5 µm as described in the previous section. Passivation with Al pads finishing are used to enable RF probing, contacting the signal level trough the passivation. The contact with GND plane is enabled using 1 µm Ø / 2 µm depth Via in the dielectric between Signal and ground plane (see Fig. 3). The GND, Via and Signal layers were all processed by single damascene on 300mm wafers. Pictures taken at different stage of the process can be seen on Fig. 4.

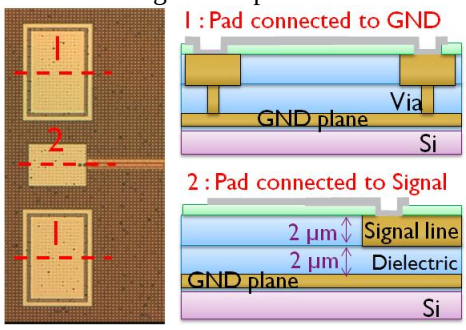

Fig. 3 Top and X-section overview of RF µStrip concept for fat damascene wires technology development and characterization.

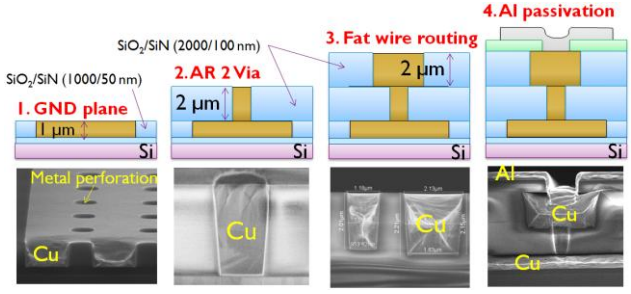

Fig. 4 µStrip Cu Ground - via - fat line damascene processing.

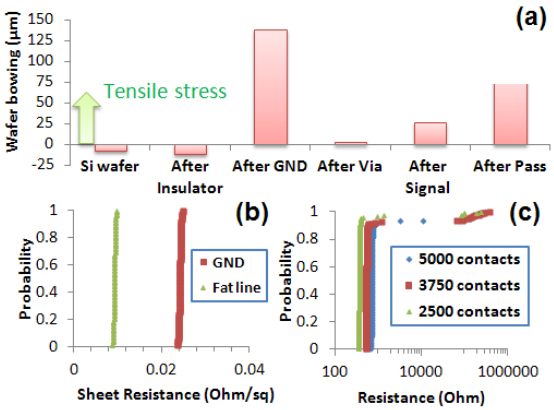

Fig. 5 Bowing measured after the different modules completion on 300mm wafers (a), GND – Fat line (Signal) sheet resistance (b) and GND/Via/Signal daisy chains electrical measurements (c).

GND plane (80% of Cu density) induces a large bowing of around 130 µm (tensile stress – Fig.5(a)). The use of a 2 µm thick compressive oxide layer compensates the stress after via processing (0.2% Cu density) and allows for reasonable bowing after fat metal layer and after passivation. Sheet resistance of the GND plane and signal lines of 195 and 94 mΩ/□ were respectively measured using Van Der Pauw structures (Fig.5(b)). The corresponding conductivity (≈5.2 x10^7 S/m) is very close from the value taken in the model. In order to check contact to GND continuity, daisy chains were qualified Fig.5(c). A yield superior to 90% was measured up to 5000 contacts. 1 and 2.6 mm µStrip lines of 3 µm width were qualified up to 50GHz (Fig. 6). Low losses of 1.24 dB/mm were measured 50 GHz with a corresponding characteristic impedance of ≈ 50 Ω.

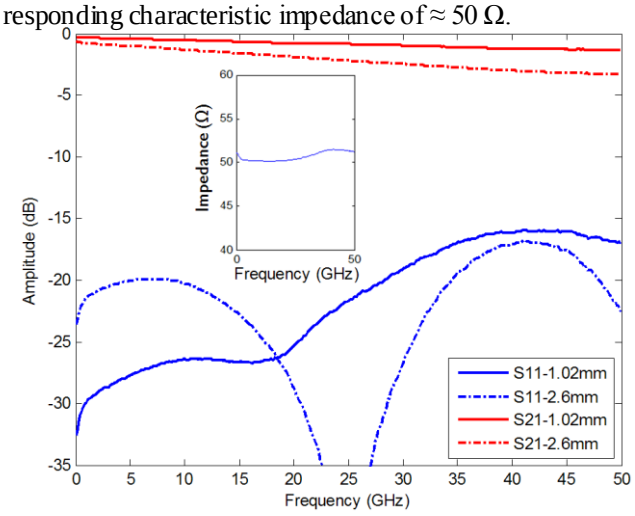

Fig. 6 RF characterization of 1 and 2.6 mm µStrip lines (3µm width) up to 50 Ghz. Extracted TFML characteristic impedance based on measurement of 1mm line is given in insert.

4. Conclusions

Based on modeling input, fat wires with low loss of 1.24 dB/mm at 50 GHz with characteristic impedance of ≈ 50 Ω were processed by damascene for interposer applications.

References

[1] K. Zoschke, ECTC (2011) 836.
[2] H. Y. Li, EPTC (2011) 341.