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Scaling of Channel Length for Highly Conductive Silicon Nanocrystal Films

Susoma Jannatul Ferdous, Yoshifumi Nakamine, Tetsuo Kodera,
Koichi Usami, Yukio Kawano and Shunri Oda

Quantum Nanoelectronics Research Center, Department of Physical Electronics, Tokyo Institute of Technology
2-12-1 Ookayama, Meguro-ku, Tokyo 152-8852, Japan
Phone: +81-3-5734-2542 E-mail: susoma.j.aa@m.titech.ac.jp

1. Introduction

Silicon nanocrystals (SiNCs) draw a lot of attention to the researchers because of their unique quantum mechanical electrical and optical properties, room temperature fabrication, and potential for low cost mass production. There are many promising applications of SiNCs based devices, such as single electron transistors, light emitting devises, optical interconnections, , electron emitters, flexible display devises RFIDs and solar cells [1]. However, SiNCs based devices are suffering with very poor electrical conductivity due to high surface reactivity of SiNCs. Firstly, a natural oxide layer is formed on the surface of SiNCs. Electron transport in the film of SiNCs ensemble is due to multiple tunneling through the surface oxide layers. The tunneling probability decreases significantly when the number of tunnel barrier increases [1-4]. Secondly, SiNCs tend to aggregate and form large clusters, which prevent from formation of closely packed array of SiNCs resulting in voids in the film. This problem was partially solved by using surface modification by HMDS treatment [5].

In order to investigate the first issue, we prepared samples of SiNC films with various electrode distances (channel length L) which means with various number of tunneling barriers, and measured electrical transport characteristics.

2. Experimental

Figure 1 shows schematic diagram of crosssectional device structure. Using Very High Frequency (VHF) remote-plasma enhanced chemical vapor deposition (CVD) system, we are able to fabricate SiNCs with a diameter of 10±1 nm which are quite uniform in size [1,3,4].

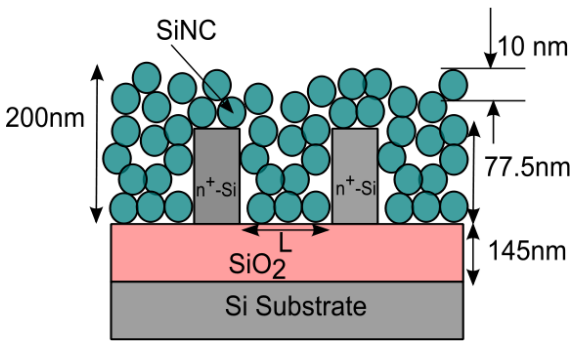

Fig. 1 Schematic diagram of device structure (cross-section view). Channel length L is varied between 20-200 nm.

Using high resolution electron beam lithography system we fabricated inter-digital electrode, as shown in Fig. 2, with channel length L varied between 20 nm and 200 nm. To make shorter channel length for the inter-digital electrode, we used reactive Cl-based ion-etching directly after EBL pattern transfer where resist was used as a mask. Fig. 3 shows the SEM image of device structure. We obtained very successful pattern where the two electrodes are perfectly electrically isolated from each other.

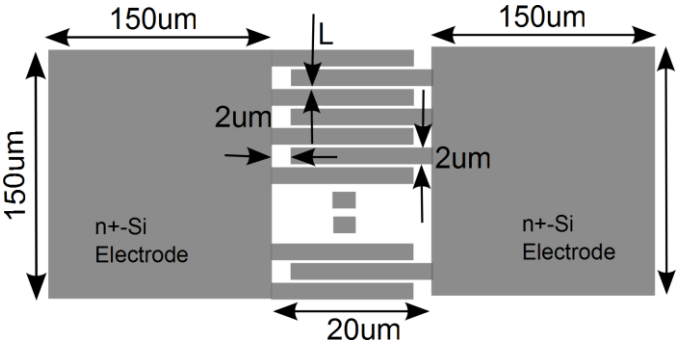

Fig. 2 Schematic diagram of inter-digital electrode (top view).

Here, highly P-doped ($1x10^{20}$ cm^{-3}) Si-electrode was used to establish Ohmic contact between the electrode and SiNCs. Besides that, high temperature treatments can be easily applicable for Si electrode for further improvement of the device. For example, high temperature annealing process to make the film more compact, surface modification of SiNCs to protect SiNCs from further natural oxidation.

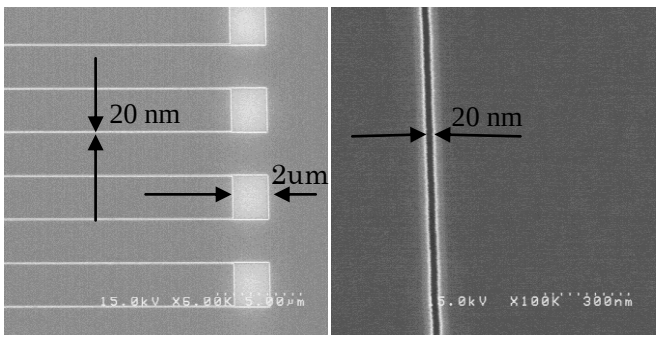

Fig. 3 SEM image of inter-digital electrode (top view) for device with L = 20nm. Dark area is Si, white area is gap (left). Magnified view of the electrode gap of 20 nm (right).

3. Results and discussion

Figure 4 shows current-voltage characteristics for SiNC films with channel length L of (A) 200 nm, (B) 80 nm, (C) 40 nm and (D) 20 nm. Electrical conductivity increases dramatically with decreasing L. While the sample (A) L = 200nm shows current level of pA range, the sample (B) with L = 80nm shows mA range. Electrical conductivity for device (A) with L = 200 nm is 4.2×10^{-10} S/cm, while that of sample (B) with L = 80 nm is 1.66×10^{-2} S/cm which is considerably higher. This result indicate that the sample with shorter L, i. e., with fewer number of tunnel barriers, shows higher transport property. If we assume that the diameter of SiNC is 10nm and aligned closely packed structure, the average number of tunnel barrier for L = 200 nm is 19, and that for L = 80 nm is 7.

As shown in Fig. 4, by further scaling the current increases for sample (C) with L = 40 nm but not significantly. In sample (D) with L = 20 nm, the current even decreases, contrary to the expectation. The mechanism of this behavior can be explained by the model described in Fig. 5. For the convenience of observing the position of electrodes, we employ the height of the electrodes as 77.5 nm in this measurement. When the aspect ratio AR (height/length ratio) of the electrode gap exceeds one, it becomes very difficult for SiNCs to fill the electrode gap. For the sample with L = 20nm, where AR = 4, even cavity is formed as is schematically shown in Fig. 5(c). This is the reason why the current for sample (D) decreases in Fig. 4. For the sample with L = 40 nm, where AR = 2, there are many voids in the channel, which results in current fluctuations in these samples. In order to solve this problem, the design of electrodes with AR of less than one might be helpful to fill the channel. However, crystal size and effective channel high should be taken into account.

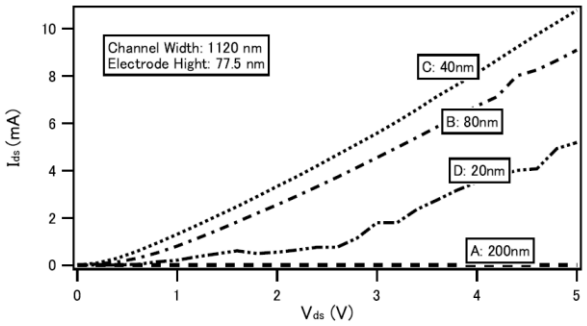

Fig. 4 *I-V* characteristics for device with L = 200nm, 80nm, 40nm and 20nm.

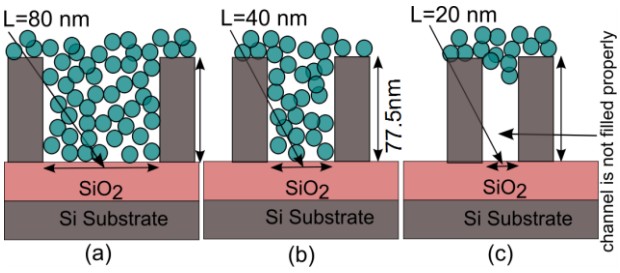

Fig. 5 Schematic model of devices with different channel length L

Time dependent electrical measurement for device with L = 40 nm (Fig. 6) shows that, conductivity decreases gradually with time because of natural oxidization of SiNCs due to high surface reactivity of SiNCs. Making an isolation layer over the SiNCs film to prevent further natural oxidization or surface modification of SiNCs is needed to keep the high conductivity.

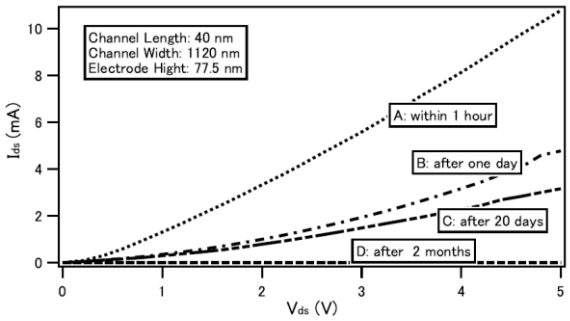

Fig. 6 Time dependent *I-V* characteristics for device with L = 40nm.

4. Conclusion

By the electrical transport measurement of the SiNCs (10 nm in diameter) films with various channel length, it was proved that conductivity of SiNCs films was determined by multiple tunneling processes. With decreasing the number of tunnel barriers, the current increases significantly. Scaling the channel length beyond the aspect ratio exceeds one, the problem of voids formation arises, which results in decreased current.

Conductivity degrades with time because of the high surface reactivity of SiNCs. Surface modification is necessary to protect SiNCs surface from further natural oxidation in order to keep the high performance of device,

References

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