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Fabrication and Characterization of MFIS Capacitor Structure with Ferroelectric (Bi,Pr)(Fe,Mn)O_3 Thin Films

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1. Introduction

Ferroelectric random access memories (FeRAM) are widely used for various mobile and portable devices because of non-volatile, high-speed operation, and low-power consumption. Available FeRAM device was composed with 1-transistor and 1-ferroelectric capacitor (1Tr-1C). In general, using the 1Tr-1C structure, it is not easy to increase the data storage density. On the other hand, ferroelectric field effect transistor with metal/ferroelectric/insulator/semiconductor (MFIS) structure has potential advantages for reducing the memory cell size compared with 1Tr-1C FeRAM, since the ferroelectric gate area was can be scaled down in proportion to FET device size[1-3].

In addition, in recent FeRAM device applications, Pb-free and high-T_c ferroelectrics are required for developments of environmental friendly material and high temperature data retention. For these requirements, Pb-free ferroelectric $BiFeO_3$ (BFO) which indicates high-T_c (~850 ˚C) compared with conventional ferroelectrics, has been studied as promising candidate for FeRAM devices[4-6].

In the present work, we report on the preparation of Au/(Pr, Mn)-codoped BFO (BPFM)/SiO_2/Si MFIS capacitor structure and characterization of electrical properties. Here, (Pr, Mn)-codoping was used to reduce the leakage current of BFO film[7,8].

2. Experimental

p-type Si (*p*-Si) substrates were cleaned by wet-chemical solution, and then dipped in a diluted HF solution for removing the native oxide layer. After the HF dipping treatment, to prepare insulating oxide layer, substrate was annealed at 1000˚C for 3 min in mixed gas (N_2:O_2 = 3:1) flow. Thickness of prepared oxide layer was 2 nm.

BPFM films were prepared on the SiO_2/Si structure by chemical solution deposition. Precursor solution with composition of $(Bi_{0.9}Pr_{0.1})(Fe_{0.97}Mn_{0.03})O_x$ was coated on the substrate by spin-coating method. Then, the films were dried at 240 ˚C for 5 min and fired at 350 ˚C for 10 min in air. These processes were repeated several times until the film thickness of BPFM became approximately 200 nm. Finally, the BPFM film was crystallized at 550˚C for 15 min in N_2 flow. All thermal treatments for BPFM films were performed by rapid thermal annealing furnace (ULVAC MILA-3000).

The crystal structure of specimen was examined by X-ray diffraction (XRD; Shimadzu XD-D1) with Cu Kα radiation. The film thickness was determined by spectroscopic ellipsometer (J.A.Woollam). Au top electrodes were deposited by thermal evaporation on the surface of BPFM film, resulting in the MFIS capacitors structure. The capacitance-voltage (*C-V*) properties were measured by LCR meter (Agilent HP4284A) with measurement frequency of 1 MHz at room temperature.

3. Results and Discussion

Figure 1 shows the XRD pattern of BPFM/SiO_2/*p*-Si structure. As shown in the figure, BPFM film has a polycrystalline perovskite phase without any impurity phases and is randomly oriented on SiO_2/*p*-Si substrate.

Figure 2 is the *C-V* curve of Au/SiO_2/*p*-Si structure with measurement frequency of 1 MHz. The curve does not show a hysteresis behavior due to charge trapping or injection although the slight flat band voltage shift was found. This result indicates that fabricated SiO_2 film is suitable for insulating layer in the MFIS capacitor structure.

Figure 3 shows the typical *C-V* curves of Au/BPFM/SiO_2/*p*-Si MFIS capacitor structure with measurement frequency of 1 MHz. As can be seen from the figure, the curves have hysteresis loops with a clockwise direction as indicated allows. According to the principle of ferroelectric FET[1], it is considered that the observed

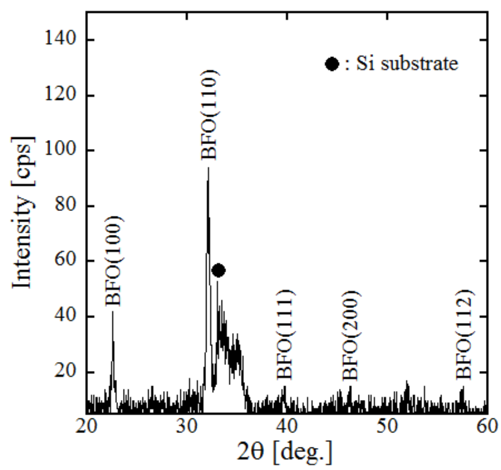

Fig. 1 XRD θ-2θ scanning pattern of BPFM/SiO_2/*p*-Si structure.

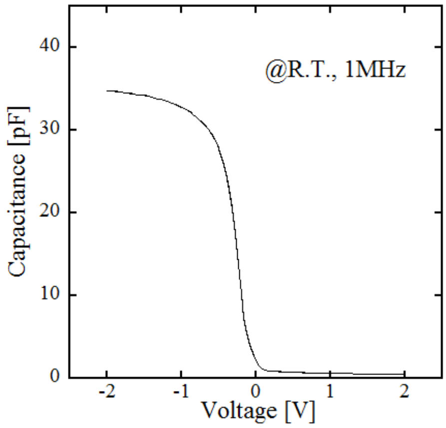

Fig. 2 *C-V* curve of Au/SiO_2/*p*-Si structure.

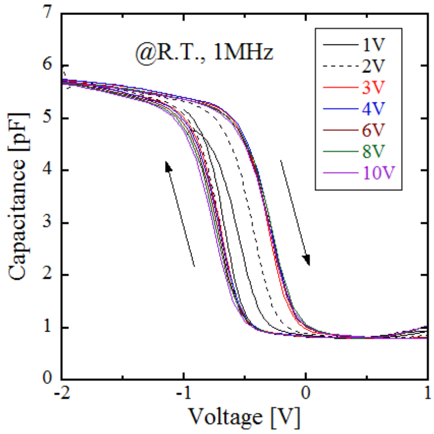

Fig. 3 *C-V* curves of Au/BPFM/SiO_2/*p*-Si MFIS capacitor structure.

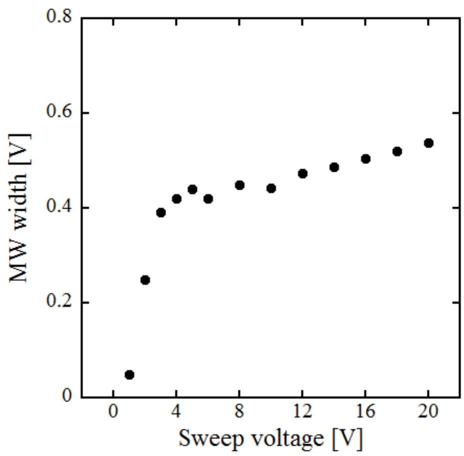

Fig. 4 MW width of Au/BPFM/SiO_2/*p*-Si MFIS capacitor structure as a function of sweep voltage.

clockwise hysteresis is caused by remnant polarization of ferroelectric gate insulator in the MFIS structure. The memory window (MW) width was approximately 0.5 V for the bias voltage sweep from -20 to +20 V.

Figure 4 shows MW width of Au/BPFM/SiO_2/*p*-Si MFIS capacitor as a function of maximum sweep voltage. With increasing the sweep voltage at low bias region (0 to 3 V), the MW width was increased quickly. Then, at higher bias region (4 to 20 V), the MW width was gradually increased although the MW width was still not saturated. This behavior is similar to the bias voltage dependence of remnant polarization of the BPFM film[7,8]. In addition, the MW width indicates simple increasing for sweep voltage, and decrease of MW width was not observed. It suggests that charge injections and trapping are not caused in the present structure[9,10]. In this regard, it can be said that the BPFM is suitable material without mutual diffusion and ionic defects formation in the present structure.

4. Conclusions

BPFM thin films were deposited on the SiO_2/*p*-Si substrates by chemical solution deposition. The polycrystalline BPFM was grown on the substrate without impurity phases. Au/BPFM/SiO_2/*p*-Si MFIS capacitor structure showed clockwise *C-V* hysteresis behavior due to remnant polarization of BPFM. The MW width in the *C-V* curve was approximately 0.5 V for the bias voltage sweep from -20 to +20 V.

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