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A 2.8 μm pixel-pitch 55 ke⁻ Full-Well Capacity Global-Shutter CMOS Image Sensor Using Lateral Overflow Integration Capacitor

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1. Introduction

Recently, a global-shutter (GS) operation is strongly desired in CMOS image sensors (CISs) in addition to a high sensitivity, a high full-well capacity (FWC) and a high resolution performance. Several GS CISs with low dark current and reset noise reduction capability have been reported [1, 2]. However, since the FWC of these image sensors is limited by a storage capacitance in the pixel, a low dark current performance and a high FWC performance have not been achieved simultaneously. A high FWC performance and wide dynamic-range GS CIS with dual storage node using the extra in-pixel capacitor together with the floating diffusion (FD) has been reported [3]. Because this GS CIS uses the FD node as high intensity signal storage, this image sensor is unable to shrink pixel-pitch by FD sharing and an issue still remains in the tradeoff between high FWC and conversion gain. Meanwhile, CIS with lateral overflow integration capacitor (LOFIC) have achieved a high sensitivity and a high FWC performance in one exposure period by solving the tradeoff between high FWC and conversion gain. In addition, it has achieved a high resolution performance keeping the high area efficiency of the FWC by using a FD sharing [4, 5].

This paper presents a GS CIS with the high area efficiency capacitor using the LOFIC technology and the pinned diffusion capacitor for the low dark current storage node. This image sensor achieves both a high FWC performance by the LOFIC and a low dark current performance by the storage capacitor simultaneously. The fabricated chip achieves a 2.8 μm pixel-pitch by using FD sharing with four pixels, about 55 ke⁻ FWC and 48.9 e⁻/sec dark current at 25°C.

2. Image Sensor Structure and Pixel Operation

Fig. 1 shows the schematic diagram of the pixel circuit. Each pixel has a pinned photodiode (PD), a transfer switch (T), a PD reset switch (P), a LOFIC, a FD, a FD connecting switch (F), a LOFIC connecting switch (S), a reset switch (R), a source follower amplifier (SF), a row select switch (X) and diffusion storage capacitor (C_{SD}) and a LOFIC. The SD connected by T, S and F is used as the storage node for the GS operation. Fig. 2 shows the potential diagram of the line A-A' and B-B' shown in Fig. 1. Potentials under the gate of the T and the S are adjusted so that the saturated photoelectrons overflow from PD to SD and from SD to LOFIC in each exposure period. The potential barrier under the gate of F is made higher than those of the T and the S in order to overflow saturated photoelectron from the SD to the LOFIC selectively. The overflow-path without the FD makes both a reset noise reduction and a pixel sharing possible. Moreover, the complete charge transfer from the SD to the FD is achieved by introducing the potential difference between the SD and the FD.

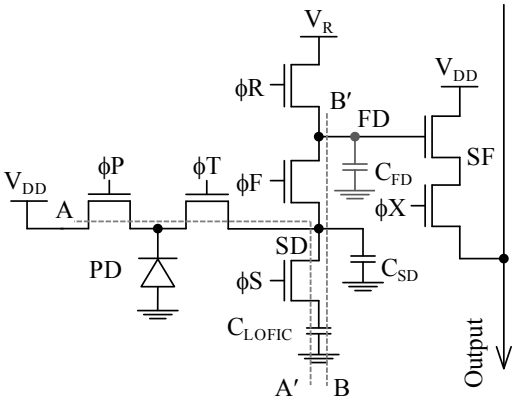

Fig. 1 Schematic diagram of the pixel circuit.

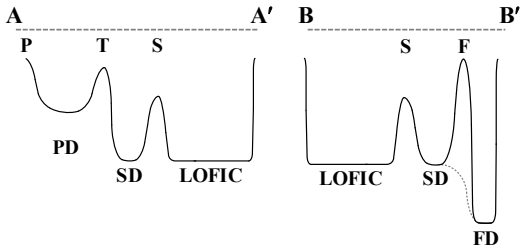

Fig. 2 The potential diagram of the line A-A′ and B-B′

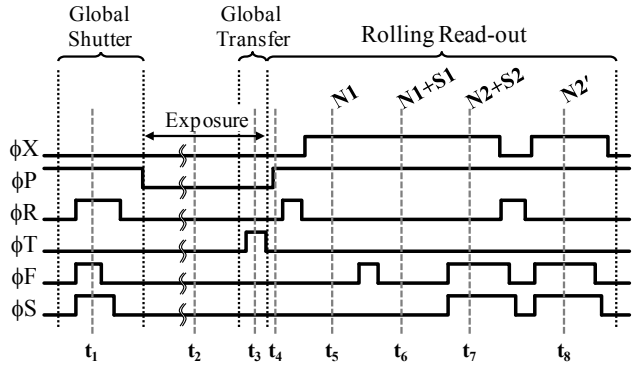

Fig. 3 The timing diagram of the pixel operation.

In this image sensor, the high capacity LOFIC for the FWC and the photodiode and the storage node for the dark current performance are designed independently. Moreover, like conventional LOFIC CISs, even if FD capacity is made small for high sensitivity performance, this CIS can secure high FWC. Benefiting from the above structure, the GS CIS achieves high sensitivity, high FWC performance and low dark current performance simultaneously.

Fig. 3 shows a timing diagram of the pixel operation. At first PD and LOFIC of each pixel are reset simultaneously for the GS operation (t_1). During the exposure period, the saturated photoelectrons of the PD overflow to the LOFIC

through the T, SD and S, and are accumulated at the SD and the LOFIC (t_2). After the end of exposure period, the T of all the pixels is simultaneously turned on and the photoelectrons are completely transferred from the PD to the SD (t_3). At this timing, the saturated photoelectrons of the SD overflow to the LOFIC through the S. After that, switch P of each pixel turns on simultaneously to avoid the photoelectrons generated during the read out operation (t_4). Each signal is read out using a rolling shutter (RS) operation. The FD reset noise is read out as the N1 after resetting the FD (t_5). The photoelectrons are completely transferred from the SD to the FD and the signal S1+N1 is read out (t_6). Then, all of the photoelectrons of FD, SD, and LOFIC are mixed and are read out as N2+S2 (t_7). After the reset of the FD, SD and LOFIC, the potential is read out as the N2′ (t_8). After the read-out operation of a row is completed, read-out operation of other rows is performed one by one until last row is read out.

4. Result

Fig. 4 shows a micrograph of the fabricated chip using 0.18μm CMOS process and the block diagram of this image sensor, and TABLE I shows the summary of the image sensor performance. Because of the introductions of the high area efficiency MOS capacitor for LOFIC and the low dark current pinned diffusion capacitor having a structure similar to a pinned PD for the storage node capacitor, this image sensor achieves the 55 ke$^-$ FWC and the 48.9 e$^-$/sec dark current at 25°C. Moreover, this image sensor achieves the 2.8 μm pixel-pitch by sharing of FD, SF, R and X by four pixels.

Fig. 5 shows the sample images of a color chart, a rotating object, a flashlight and a metronome. The light condition of the object is low in the left half and high in the right half. At Fig.5 (b), although wide dynamic range capturing can be performed in the light intensity range from a dark place to the flashlight, the distortion has occurred to the rotating object and the metronome. On the other hand, at Fig.5 (d), no distortion and artifacts are observed with wide dynamic range capturing. Fig. 6 shows the relation between the FWC per pixel area and the pixel-pitch for this image sensor, the conventional GS CISs and conventional RS CIS which have been reported recently. The GS LOFIC CIS in this work has achieved the FWC performance higher than conventional GS CISs by one order and has almost the same FWC per unit area as the conventional LOFIC CIS.

5. Conclusions

A global-shutter operation CMOS image sensor introducing both the high area efficiency of lateral overflow integration capacitor for the high full-well capacity and the low dark current storage node structure for the low dark current performance has been developed and demonstrated.

References

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[4] S. Sugawa, et al., *ISSCC* (2005) 352.
[5] S. Sakai, et al., *ESSCIRC* (2009) 240.

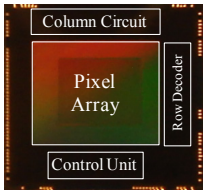

Fig. 4 A micrograph of the fabricated chip and a block diagram.

TABLE I Summary of the image sensor performance

Process	0.18μm CMOS
Supply Voltage (Analog/Digital)	3.3 V / 1.8 V
# of Effective Pixels	$1328^{(H)} \times 1029^{(V)}$
Die Size	$9.1^{(H)} \times 8.6^{(V)}$ mm^2
Pixel Pitch	2.8 μm
Maximum Frame Rate	20 fps
Conversion Gain (input referred)	43 μV/e$^-$
Dark Current @25°C	48.9 e$^-$/sec
Full Well Capacity	~55,000 e$^-$

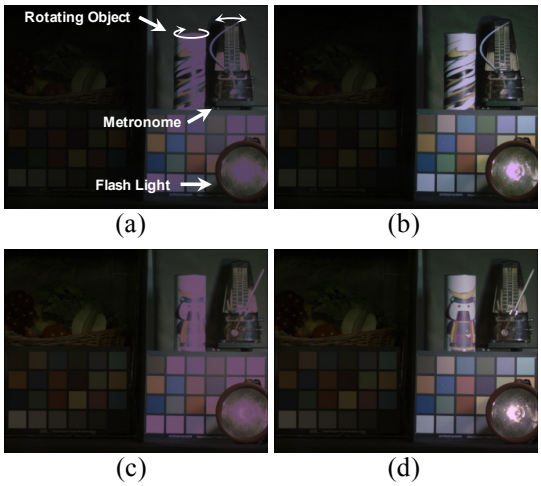

Fig. 5 The sample images of a color chart, a rotating object, a flashlight source and a metronome. (a) Conventional RS, (b) RS + LOFIC, (c) Conventional GS and (d) GS + LOFIC.

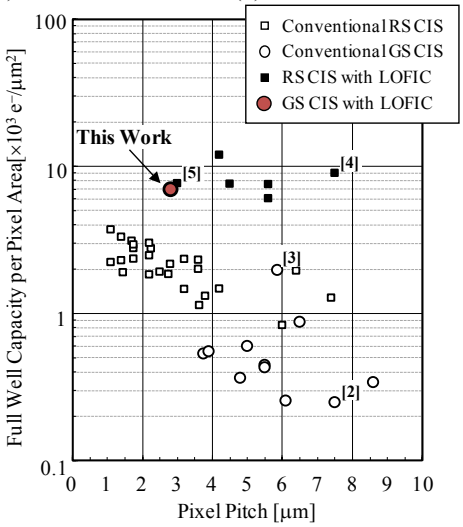

Fig. 6 The relation between FWC per pixel area and pixel-pitch.